

Cost Effective
Network Processor
for TCP/IP
with ARM7TDMI™

MLN7400
Evaluation Board Manual

Version 0.20

December 31, 2003

MCS Logic Inc.

Revision History

Version	Date	Revision Description
V 0.10	December 30, 2003	First Release

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Chapter 1 Introduction

EVB7400 is a MLN7400 evaluation board and MCS-uClinux training kit that is suitable for code development and exploration of MN7400 with MCS-uClinux. It includes much of the hardware and software required completing your application development. It supports various function related with network, communication such as IIC, SPI, UART, 10/100 Ethernet, multimedia module such as sound DAC, storage media such as NAND FLASH memory module. Using the JTAG interface, you can debug the EVB7400 directly.

1.1 System Requirements

-. Host computer : IBM compatible PC
-. EVB7400 (Evaluation Board for MLN7400)
-. DC 5V Power

JTAG
X-Tal/Osc
ARM7TDMI
4KBytes Cache
M_Bus I/F
PLL
UART0~4
IIC Serial EEPROM &RTC
SPI Serial EEPROM
DAC(CS4340)
MIC IN
KEY MATRIX
NAND Flash
Status LEDs
Exetenal Interrupt Key
Ethernet PHY (AC101L)
Boot ROM (ROM Bank0)
User Flash (ROM Bank1)
SRAM (ROM Bank2)
PCMCIA Socket (ROM Bank3)
SDRAM
10/100 Ethernet MAC
DMA
2ch GDMA
Memory Controller
M_Bus
Peripheral Bridge
Peripheral Bus
4 Console UARTs
1 high-speed UART
I2C
SPI
GPIOs
4 channel ADC
4 Timers
WDT
DAC I/F
Interrupt Controller

[Figure 1] EVB7400 BLOCK DIAGRAM

ADDRESS	MLN7400 MAP	EVB7400
0x000_0000 ~ 0x0FF_FFFF	ROM/Flash bank 0 (16Mbytes)	FLASH(512KB)
0x100_0000 ~ 0x1FF_FFFF	ROM/Flash bank 1 (16Mbytes)	SRAM(128KB)
0x200_0000 ~ 0x2FF_FFFF	ROM/Flash bank 2 (16Mbytes)	FLASH(2MB)
0x300_0000 ~ 0x3FF_FFFF	ROM/Flash bank 3 (16Mbytes)	PCMCIA Card
0x400_0000 ~ 0x5FF_FFFF	Cacheable SDRAM area (32Mbytes)	SDRAM 64Mbits(8Mbytes)
0x600_0000 ~ 0x600_5FFF (Cacheable)		
0x800_0000 ~ 0xEFF_FFFF (Non-Cacheable)		
0xF00_0000 ~ 0xFFF_FFFF	SFR Registers	

		After Remap	After SRAM Remap	
0x000_0000	ROM/Flash Bank0	DRAM	ROM/Flash Bank1	Cacheable
0x100_0000	ROM/Flash Bank1		ROM/Flash Bank0	
0x200_0000	ROM/Flash Bank2	ROM/Flash Bank0	ROM/Flash Bank2	
0x300_0000	ROM/Flash Bank3	ROM/Flash Bank1	ROM/Flash Bank3	
0x400_0000	DRAM	ROM/Flash Bank2	DRAM	
0x500_0000		ROM/Flash Bank3		
0x600_0000	Reserved	Reserved	Reserved	
0x800_0000	ROM/Flash Bank0	DRAM	ROM/Flash Bank1	Non-Cacheable
0x900_0000	ROM/Flash Bank1		ROM/Flash Bank0	
0xA00_0000	ROM/Flash Bank2	ROM/Flash Bank0	ROM/Flash Bank2	
0xB00_0000	ROM/Flash Bank3	ROM/Flash Bank1	ROM/Flash Bank3	
0xC00_0000	DRAM	ROM/Flash Bank2	DRAM	
0xD00_0000		ROM/Flash Bank3		
0xE00_0000	Reserved	Reserved	Reserved	
0xF00_0000	SFR	SFR	SFR	

[Figure 2] MEMORY MAP

1.2 Board Components

The arrangement of major components on the board is shown in Figure 3. The major components include:

[Figure 3] BLOCK DIAGRAM (TOP VIEW)

A Flash ROM

There is a socket(U9) which accept 512Kbyte size of 8 bit Flash Memory(AT29C010 ~ 40). This is for diaganostic program(includes all pheriperal device driver and TCP/IP protocol stack) and BIOS(MCS-uClinux Boot loader) program.

User Flash memory(Selectable Boot ROM)

A mounted 48 TSOP type flash(AM29LV160BB), U8, is mounted for saving MCS-uClinux image. It has 2Mbytes(1M x 16bits)size. If you want to use this for boot ROM, SW2 should be set to to X16 and U9 should be removed. (The default setting is X8)

SDRAM

SDRAM size is 8Mbytes (4M x 16bits)

SRAM

There is a SRAM at ROM Bank1. SRAM SIZE is 64K x 16 bits.

NAND Flash

A mounted NAND Flash ROM is provided for saving user data.

To use NAND flash, you should install and uninstall some 0 ohm register at bottom of board. Please refer to chapter 2 and Schemetic.

EEPROM(AT24C256, AT25040)

There are two EEPROM(U3, U4). One is an IIC Serial EEPROM(U3) and the other is a SPI serial EEPROM(U4).
The size of EEPROM(U3) is 32Kbytes, and the size of EEPROM(U4) is 4Kbytes.

RTC & Thermometer

There is a DS1629(U5) for RTC and thermometer check. The RTC clock is supplied by the crystal(32.768KHz)

Serial Port

There are 5 9-pin female Serial ports for serial data communiation. One is for console between the host PC and EVB7400 and others for converter(Serial to Ethernet, Serial to wireless and so on). And there is one 9-pin mail Serial ports for High Speed UART.

Ethernet Interface

There are RJ45 connector and Ethernet Phy for network.(AC101L, 10/100 BASE-T)

AUDIO IN/OUT

There is a stereo DAC(CS4340) for AUDIO out. And MIC and AMP is connected to ADIN3(ADC channel3) for AUDIO In.

Reset Button

There is a button for system reset.

Power On/Off Switch

There is a swithch for power on/off.

LED Indicatorst

Seven LEDs are supplied on the EVB7400. Each LED shows power status, user programmable status, ethernet link and activity.

PCMCIA Socket

There is a PCMCIA Socket(J2). To use it, you should set ROM BANK3 as PCMCIA mode.

JTAG Port

One 20-pin JTAG port(J3) is supplied to connect with JTAG based Emulator.

Expansion Connectors

Seven connectors(JP2~JP8) are supplied for system expansion. They contain board data bus, adddress bus, external memory bank control, IIC, SPI, and MII signals.

Key Matrix

There are 12 key buttons. They can be used ADC application.
Five buttons(SW4, SW7, SW10, SW13, SW15) are connected to ADIN0(ADC channel 0).

Four buttons(SW5, SW8, SW11, SW14) are connected to ADIN1(ADC channel 1).
Three buttons(SW5, SW8, SW11, SW14) are connected to ADIN2(ADC channel 2).

External Interrrupt Key
There are two button to use external interrupts. Each button(S1,S2) is connected to External interrupt0 and 2.

External Timer0 Clock
Timer0 can be supplied by the external clock(ocsillator)

Chapter 2 Board Configuration

The EVB7400 is set with default configuration. You can use the board with the defualt settings direclty. However, you can also change the settings according to your nedds.

2.1 Endian Selection (SW1)

Status	Description
BIG (switch up) LITTLE	BIG Endian
BIG (switch down) LITTLE	Little Endian

2.2 Boot ROM and ROM Bank0 length Selection (SW2)

Status	Description
X8 (switch up) X16	ROM BANK0 Size is 8 bits. ROM BANK0 : AT29C040 512 X 8bits Flash ROM BANK2 : AM29LV160BB 1M X 16bits Flash
X8 (switch down) X16	ROM BANK 0 size is 16 bits. ROM BANK0 : AM29LV160BB 1M X 16 bits Flash *Note : AT29C040(U9) should be removed

2.3 NAND FLASH

You can use NAND Flash through GPIO of MLN7400. To use NAND Flash you shoud install 0 ohm registance.
Refer to schementic page4.

Install Register reference	Unintall Register Reference
R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26	R39, R40, R41,R42, R43, R44, R54,R55,R56

*Note: To use NAND Flash, you can't use SPI Interface, Console UART3 and High Speed UART(UART4)

2.4 GPIO Setting

<128-TQFP/ 144 -LQFP Common I/O>

PIN	Shared	Initial	Board Setting	Setting Value
GP00	CUTXD1	N,I	UART1	S, O
GP01	CURXD1	N,I	UART1	S, O
GP02	CUTXD2	N,I	UART2	S, O
GP03	CURXD2	N,I	UART2	S, O
GP04	CUTXD3	N,I	UART3/NFWEN	S, O
GP05	CURXD3	N,I	UART3/NFWRN	S, O
GP06	CUTXD4	N,I	UART4/NFALEN	S, O
GP07	CURXD4	N,I	UART4/NFCLEN	S, O
GP08	nBE[0]	N,I	SRAM(nBE0)	S, O
GP09	nBE[1]	N,I	SRAM(nBE1)	S, O
GP10	TOUT[0]	N,I	Timer0 TOUT0	S, O
GP11	TOUT[1]	N,I	SPI SS#	N, O
GP12	TX_ERR	S,0	LED 0	N, O
GP13	NTRST	S,I	JTAG(nTRST)	S, I
GP14	ECSN2	S,O	SRAM(ECSN2)	S, O
GP15	ECSN3/CE1#	S,O	PCMCIA(CE1#)	S, O
GP16	SPIMISO	N,I	SPI MISO/NFCEN	S, I
GP17	SPIMOSI	N,I	SPI MOSI/NFRDN	S, O
GP18	SPICLK	N,I	SPI Clock/NFRBN	S, O
GP19	EXINT0	N,I	Ext Int0 Test	S, I
GP20	EXINT1	N,I	PCMCIA IRQ	S, I
GP21	EXT_UCLK	N,I	LED 1	N, O
GP22	REG#/DLRCK	N,I	PCMCIA REG#/DLRCK	S, O
GP23	CE2#/DBCK	S,O	PCMCIA CE2#/DBCK	S, O
GP24	IORD#/DMCK	N,I	PCMCIA IORD#DMCK	S, O
GP25	IOWR#/DDATA	N,I	PCMCIA IOWR#/DDATA	S, O
GP26	ENWAIT	N,I	PCMCIA ENWAIT	S, O

<144 -LQFP Extended I/O>

PIN	Shared	Initial	Board Setting	Setting Value
GP27	EXT_TCLK0	N,I	Ext Timer0 Clk	S, I
GP28	EXT_TCLK1	N,I	LED 2	N, O
GP29	EXT_TCLK2	N,I	LED 3	N, O
GP30	HUARTnDCD4	N,I	NFIO0	N, I
GP31	HUARTnCTS4	N,I	NFIO1	N, I
GP32(0)	HUARTnRTS4	N,I	NFIO2	N, I
GP33(1)	HUARTnDSR4	N,I	NFIO3	N, I
GP34(2)	HUARTnDTR4	N,I	NFIO4	N, I
GP35(3)	EXINT2	N,I	Ext Int2 Test	S, I
GP36(4)	EXINT3	N,I	NFIO5	N, I
GP37(5)	TOUT[2]	N,I	NFIO6	N, I
GP38(6)	TOUT[3]	N,I	NFIO7	N, I
GP39(7)	DLRCK	N,I	DLRCK	S, O
GP40(8)	DBCK	N,I	DBCK	S, O
GP41(9)	DMCK	N,I	DMCK	S, O
GP42(10)	DDATA	N,I	DDATA	S, O

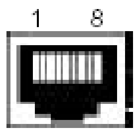
S : Special
N : Noraml
I : Input
O : Output

1) GP22 ~GP25 는 7400P 의 경우 PCMCIA 와 DAC 을 선택적으로 사용

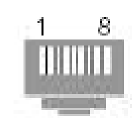
Chapter 3 Setup EVB7400 Environments

3.1 Ethernet 10/100 BASE-T Connector

Same connector and pin for both 10Base-T and 100 Base-Tx



< At the network interface card/hubs >



< At the cables >

RJ45 female connetor at the network interface cards and hubs
RJ45 male connector at the cable

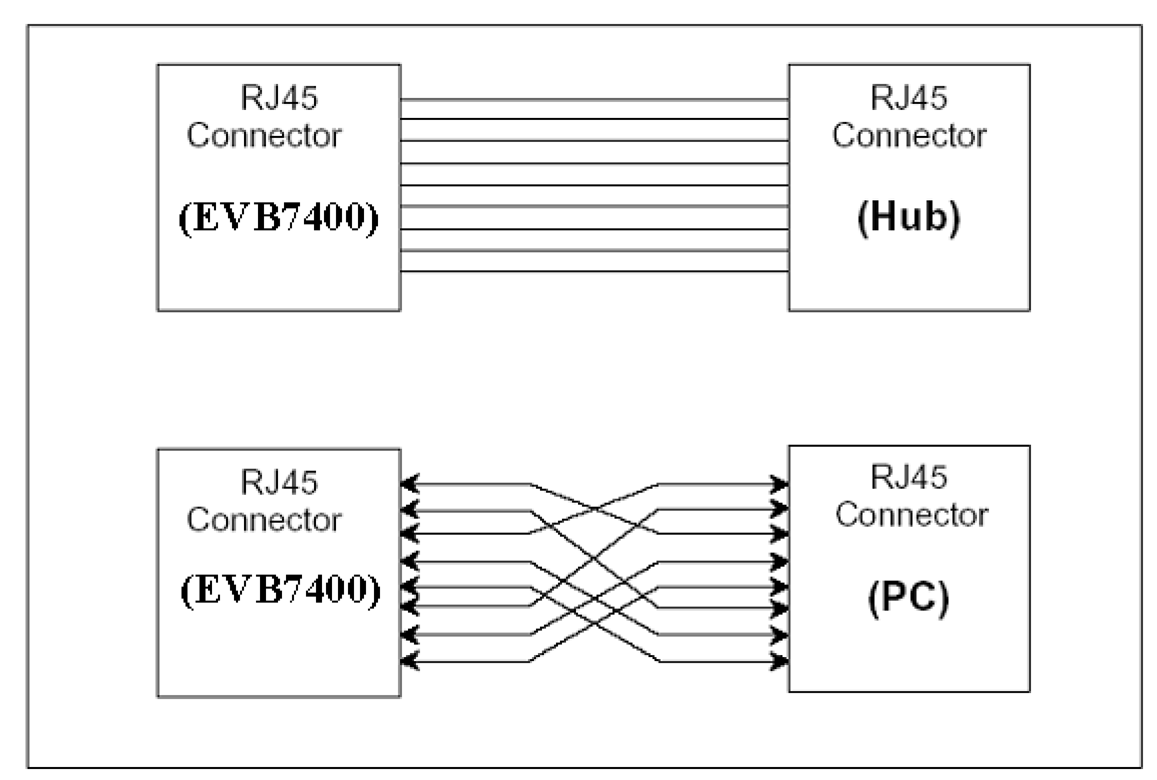
Pin	Name	Descriptions
1	TX+	Tranmit Data+
2	TX-	Tranmit Data-
3	RX+	Receive Data+
4	N/C	Not Connected
5	N/C	Not Connected
6	RX-	Receive Data-
7	N/C	Not Connected
8	N/C	Not Connected

NOTE : TX & RX are swapped on hub

3.2 Connection Method for UTP Cable

RJ45 pins on EVB7400 is defined to Adapter side. So, you straight connect EVB7400 to hub through UTP cable. In this case, between the EVB7400 and the Hub, the pin numbers correspond to each other.

Between the EVB7400 and the NIC which is on the Host PC, you have to connect each other through UTP cable which is crossover patch cord.



[Figure 4] UTP CABLE CONNECTION

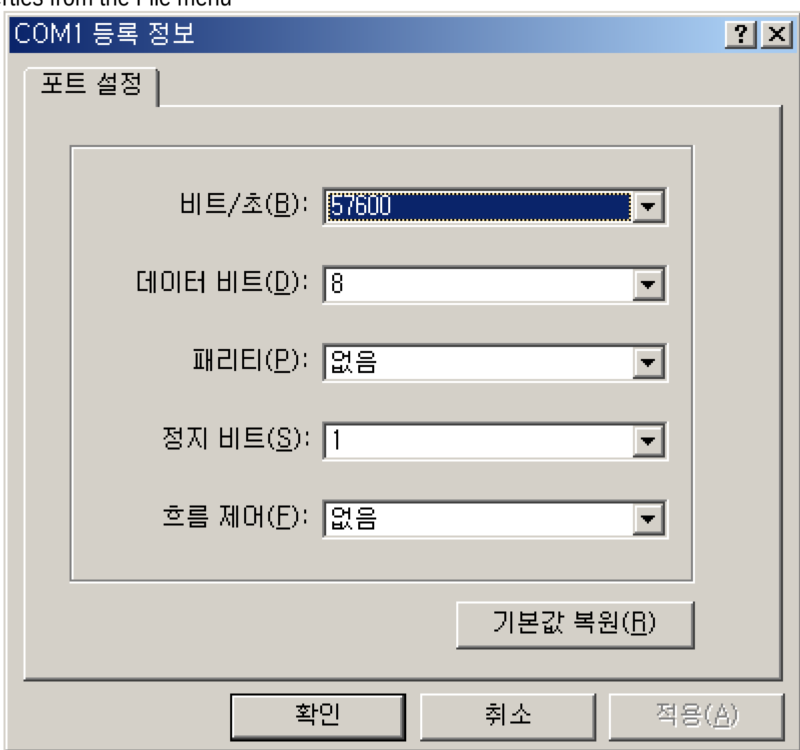
Chapter 4 Connection Configurations for Debug Console

4.1 Configuration the Hyper Terminal

To configure the Hyper Terminal, which is a Windows utility program for serial communications, refer to following steps:

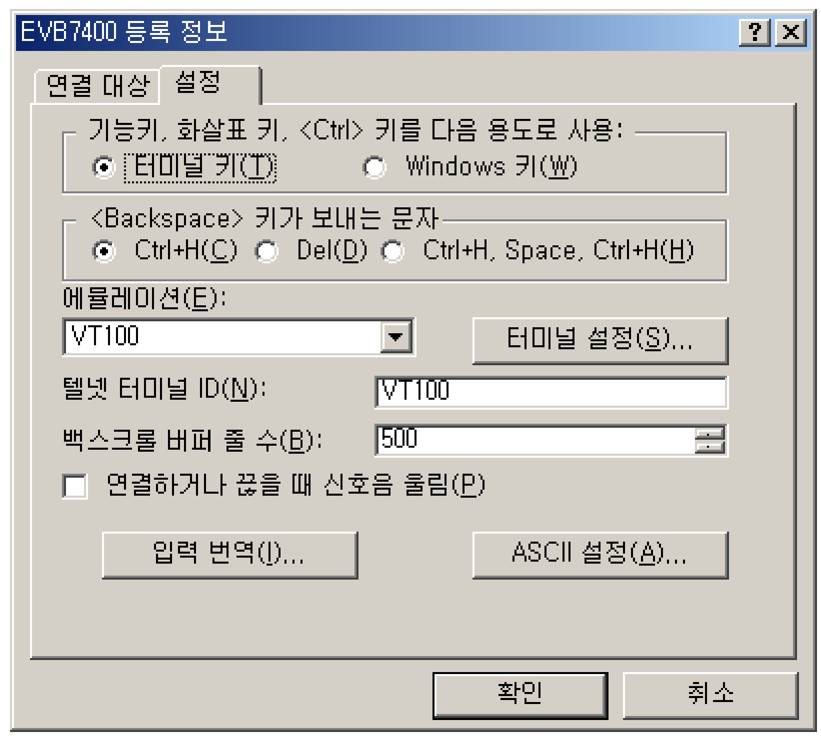
1. Run the Hyper Terminal program
   -. Window 95/98/2000/XP start tool bar -> Program -> Accessories -> Hyper Terminal Group
   -> Double click Hyperterm.exe -> Enter a connection name -> Select a icon -> Click OK.
2. Select COM Port to communicate with EVB7400 board.
   -. Choose COM1 or COM2 as the serial communication port and click OK.
3. Set the serial port properties
   -. Bits per second: 57600 bps
   -. Data Bits : 8 bits
   -. Stop Bits : 1
   -. Flow control : None

4. Select the Properties from the File menu



[Figure 5] PROPERTIES SETTING PAGE

5. Choose Setting Page.



[Figure 6] CHOOSE SETTING PAGE

6. Re-connect Hyper Terminal to run at new properties
   Disconnect : Call -> Disconnect
   Connect: Call -> Call
7. Power-On Reset or push the reset button on EVB7400 board
   Now, the diagnostic program menu is showed on the Hyper Terminal

4.2 Downloading Binary Image and Flash Write

4.2.1 Downloading Binary Image

You can download a binary image file through the serial cable to target without an emulator.

1. Type “ f ” to download user program to EVM7400 on Diagnostic program main menu.

```
MLN7400 - 하이퍼터미널
파일(F) 편집(E) 보기(V) 호출(C) 전송(T) 도움말(H)

        ---    MCS Logic inc. Network and Communucation team    ---

                 TCP/IP Stack Diagnostic Program for MLN7400
                      Date 2004.1.28   Version 0.96

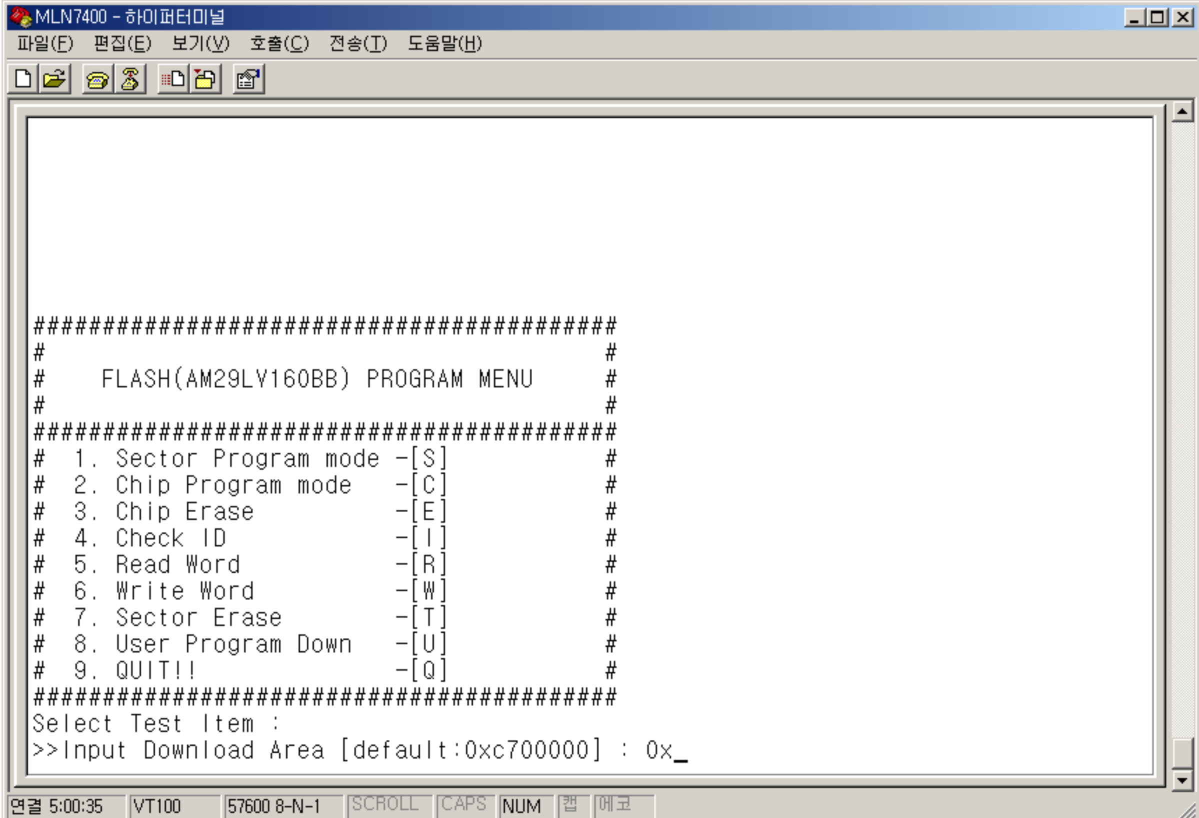
     1. TCP/IP Protocol Stack Test         a. General Purpose I/O Test
     2. Network Configuration              b. Timer Test
     3. Ethernet Controller Test           c. Memory Test
     4. Console Uart Test                  d. External Interrupt Test
     5. IIC Controller Test                e. RTC(DS1629) Test
     6. SPI Controller Test                f. Flash(AM29LV160BB) Program
     7. Cache On/Off                       g. ADC Test
     8. GDMA Test                          h. DAC Test
     9. View System Configuration
     0. Show Menu

 Select Test Item :  _

                                   17-02-2004(Tuesday)    11:26:25

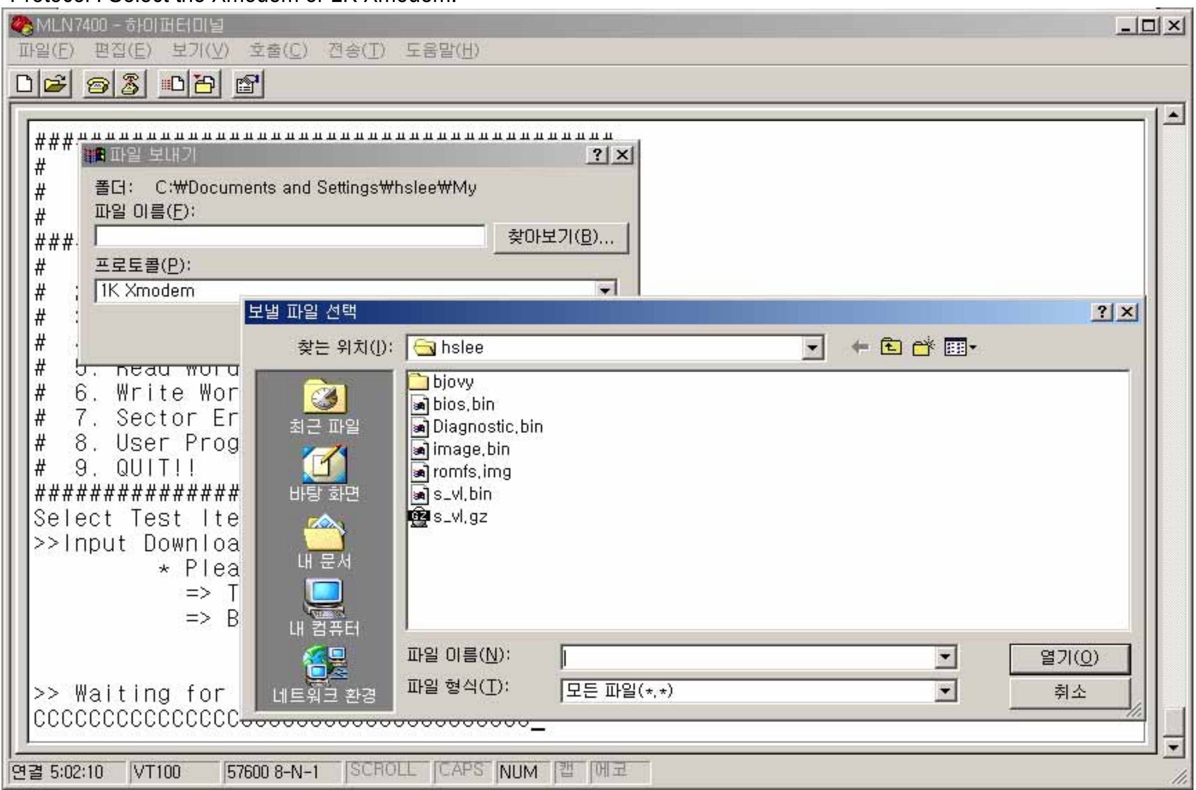
연결 4:57:48   VT100   57600 8-N-1   SCROLL   CAPS   NUM   캡   에코
```

2. Type "8" at Flash Program Menu and type address to download.

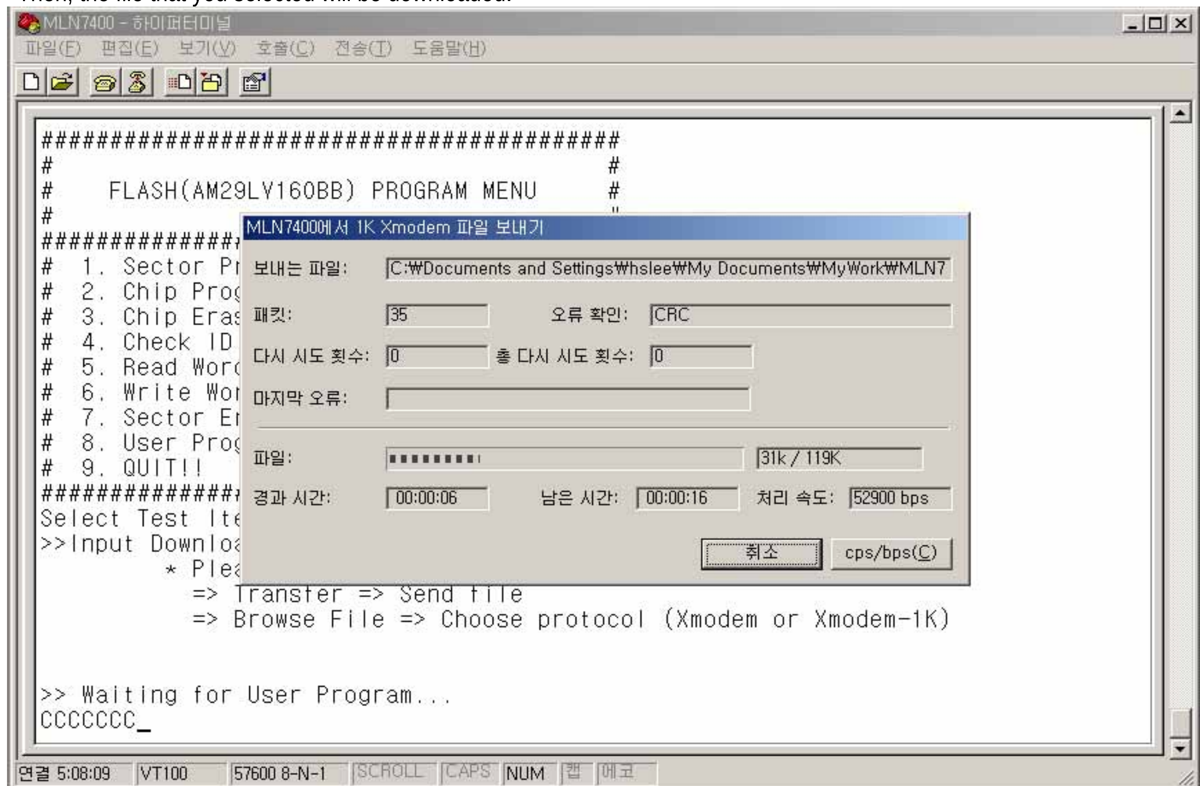




3. select the Send File from the Transfer menu
File Name : Select the file name, which you want too download.
Protocol : Select the Xmodem or 1K Xmodem.



4. Click Ok.
Then, the file that you selected will be downloaded.



4.2.2 Flash Write

You can write downloaded binary image at User flash memory(AM29LV160BB, U8).

Type “2” to write an executable binary file at User Flash memory.
Then, you can execute your image by changing Boot Rom selection switch(SW2) to X16(default is X8).

MLN7400 - 하이퍼터미널

파일(F) 편집(E) 보기(V) 호출(C) 전송(T) 도움말(H)

```
##########################################
#                                        #
#    FLASH(AM29LV160BB) PROGRAM MENU     #
#                                        #
##########################################
#   1. Sector Program(64KB)-[S]          #
#   2. Chip Program mode   -[C]          #
#   3. Chip Erase          -[E]          #
#   4. Check ID            -[I]          #
#   5. Read Word           -[R]          #
#   6. Write Word          -[W]          #
#   7. Sector Erase        -[T]          #
#   8. User Program Down   -[U]          #
#   9. QUIT!!              -[Q]          #
##########################################
Select Test Item :
Flash full Programming is started!!!!
[ID Check]
Manufacture ID=   1(0x0001), Device ID(0x2249)=2249
[Flash full Erase]
Chip Erase is started!!! : _
```

연결 2:58:06 | VT100 | 57600 8-N-1 | SCROLL | CAPS | NUM | 캡 | 에코

Chapter 5 Opennice32 Installation

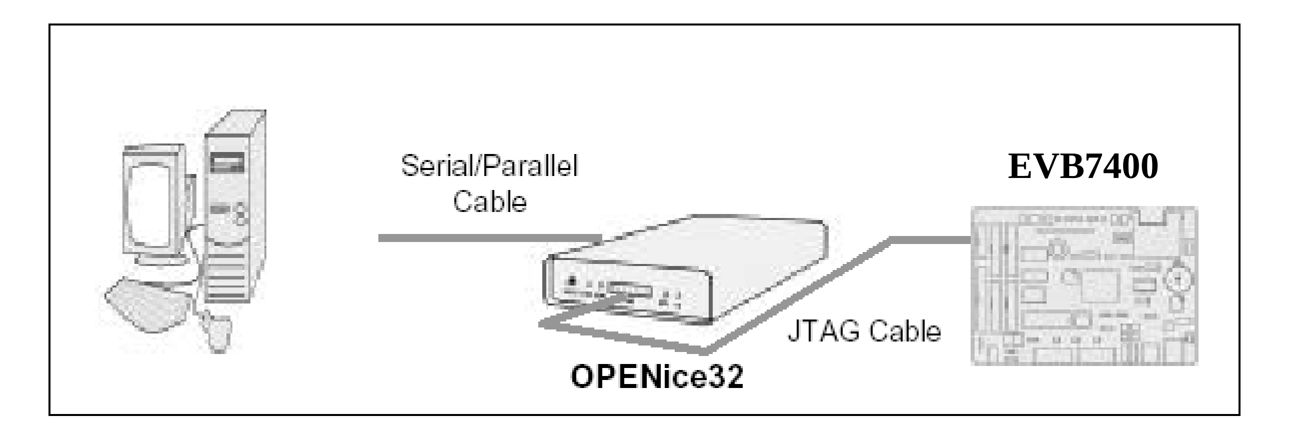
5.1 OPENice32

The OPENice32 can also be connected with the EVB7400 as a debugging system for software applications development. OPENice32 is a JTAG-based, nonintrusive, debugging system for ARM-based controllers or processors. JTAG provides the interface between a debugger and the ARM-based controller development board.

To use the OPENice32, the following additional equipment are required:
- OPENice32
- 14-way ribbon cable
- 9-pin RS232 cable or parallel cable
- 5 V DC (Max. 3A) power supply

5.2 Connecting EVB7400 and PC

The OPENice32 should be connected to the EVB7400's JTAG Port (J3) via a 20-way cable, and to the host PC via a 9-pin RS232 serial or parallel cable.
To power on the OPENice32, DC 5 V power supply is required.



[Figure 7] CONNECTING WITH OPENICE32

5.3 Powering up the Board and OPENice32

We recommend that you power on the EVB7400 before the OPENice32 is powered on. In this way, the system initialization and memory configuration for EVB7400 performed by the Boot Code can be completed first.
Otherwise, it may cause the failure of code download via JTAG.

Chapter 6 EVB7400 1.0 Schemetic and BOM

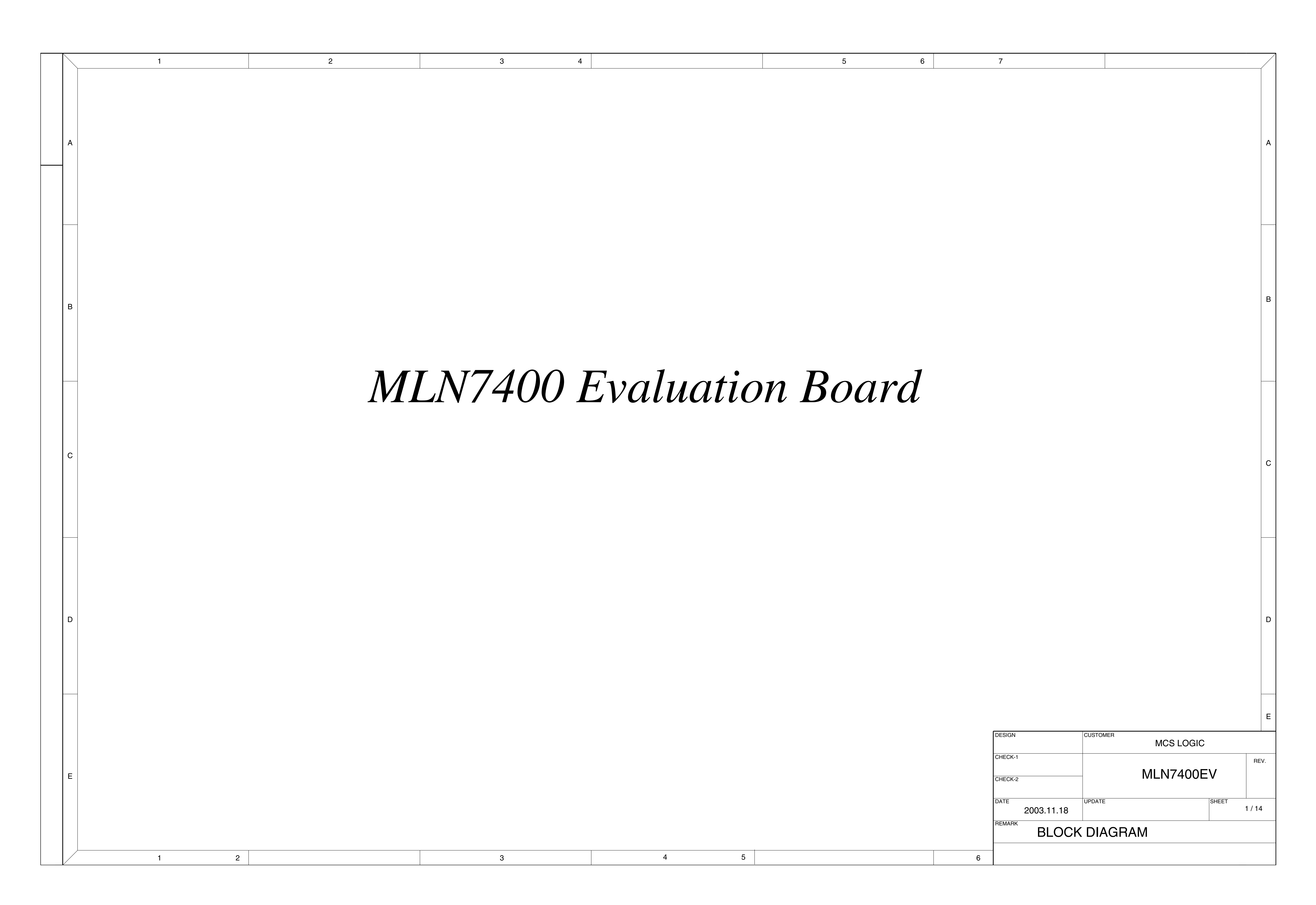
6.1 EVB7400 BOM

No.	PART NO	GEOMETRY	COUNT	DESCRIPTION	REFERENCE	Vendor
1	MLN7400	144LQFP	1	Microprocessor	U1	MCS Logic
2	MLN7400P	128TQFP	1	Microprocessor	U2	MCS Logic
3	AT24C256	8 SOIC	1	EEPROM(IIC)	U3	Atmel
4	AT25040	8 SOIC	1	EEPROM(SPI)	U4	Atmel
5	DS1629	8 SOIC	1	RTC	U5	Dallas
6	K6R1016V1D	44TSOP	1	SRAM	U6	Samsung
7	K4S641632	54TSOP	1	SDRAM	U7	Samsung
8	AM29LV160BB	48TSOP	1	Flash	U8	AMD
9	AT29C040A	32DIP	1	Flash	U9	Atmel
10	AC101L	48 TQFP	1	PHY	U10	Altima
11	H1102		1	Transformer	U11	PULSE
12	MAX3232	16 SOIC	3	RS232	U12, U13, U14	MAXIM
13	74LVC14		1		U15	
14	74LV08		1		U16	
15	AMS1086		1	Regulator	U17	semtech
16	MAX4468EKA	8pin SOT23	1	AMP	U18	MAXIM
17	CS4340	16 SOIC	1	Stereo DAC	U20	CRYSTAL
18	K9F2808-YCB0	48 TSOP	1	NAND Flash	U21	Samsung
19	Xtal_osc 10MHz	Half	1	Xtal-Oscillator (System CLK)	X2	
20	Xtal_osc 25MHz	Half	1	Xtal-Oscillator (PHY CLK)	Y2	
21	Crystal 32.768KHz	DIP(cylinder type)	1	Crystal(RTC)	Y1	
22	Crystal 10MHz	DIP(ATS Holder type)	1	Crystal (System CLK)	X1	
23	Xtal_oxc 1MHz	Half	1	Test CLK	X3	
24	Battery	CR2032	1	3V coin Battery	BT1	
25	Battery Connector		1			
26	PushButton SW		15	Reset, ExtInt	S1,S2,S3,SW4,SW5, SW6,SW7,SW8,SW9,SW10,SW11, SW12,SW13,SW14, SW15	
27	DPDT SW		3		SW1,SW2,SW16	
28	Power Toggle SW	3pin DIP	1	A12AP	SW3	NKK
29	1N4004	DIP	2	Diode	D1,D2	
30	1N4148	SMD	1	Diode	D3	
31	LED		5		D4,D5,D6,D7,D8	
32	PCMCIA 68Pin Con		1	ICM-C68H-S112-400N1	J2	JST
33	RJ-45		1		J1	
34	HEADER 10X2		1	JTAG	J3	
35	POWER JACK		1	DC5V PWR	J4	
36	MIC IN JACK		1		J5	
37	AUDIO OUT JACK		1		J6	

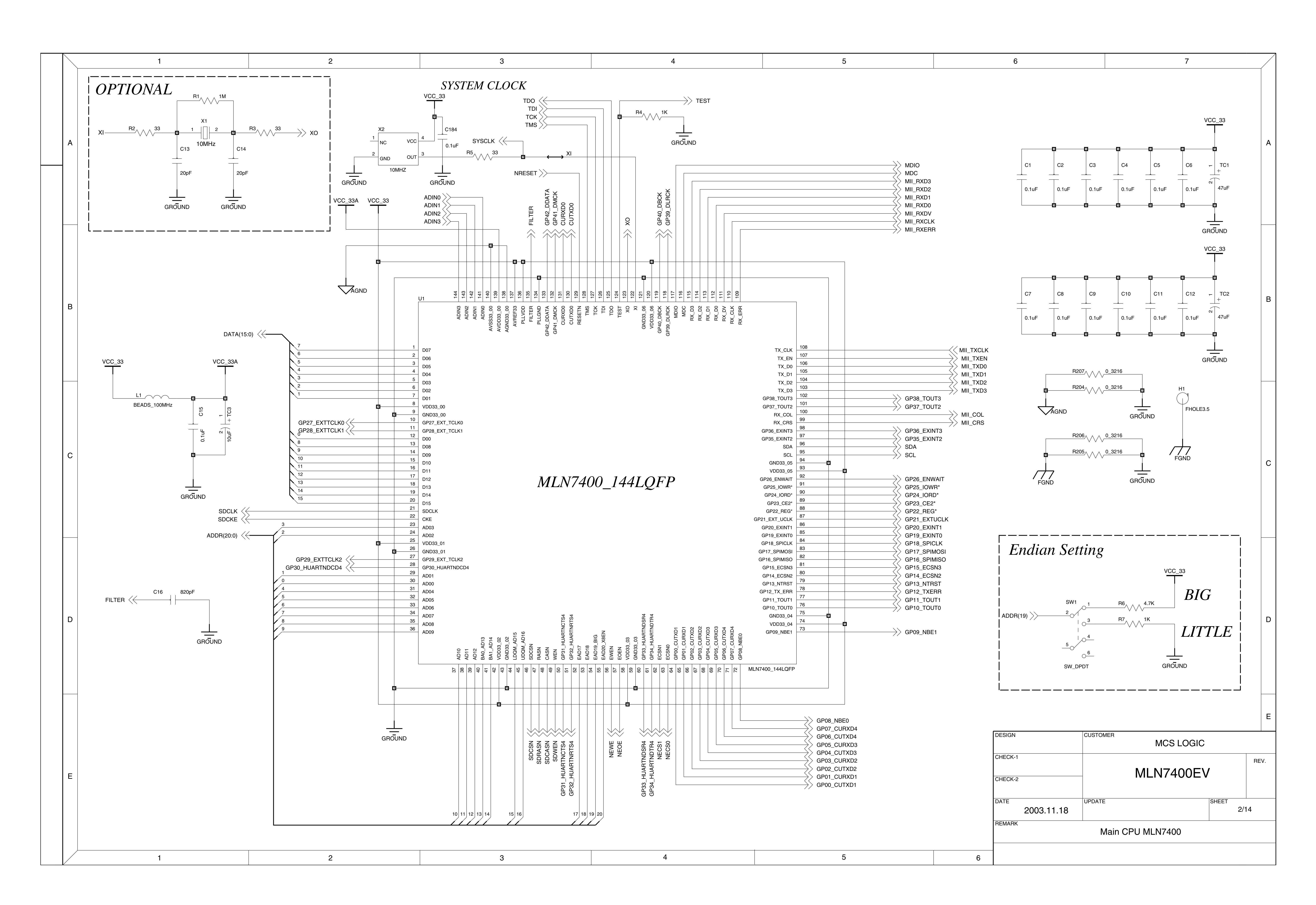
38	DB9 FEMAIL		5	UART0~4	P1,P2,P3,P4,P5	
39	DB9 MAIL		1	HUART Option	P6	
40	HEADER 13X2		4	DATA, MII, ADDRESS, MEMORY	JP3,JP4,JP6,JP8	
41	HEADER 24X2		1	GPIO heaser	JP7	
42	HEADER 4X2		1	IIC & SPI	JP2	
43	HEADER 6X2		1	HUART header	JP5	
44	HEADER 1		7	Test Pin	JP1,TP1,TP2,TP3,TP4 TP5, TP6	
45	Beads(100Mhz)	2012	1	L	L1	
46	0	0603(1608)	68	R	R8,R9,R10,R11,R12, R13,R14,R15,R16,R17, R18,R19,R20,R21,R22, R23,R24,R25,R26,R27, R28,R29,R30,R31,R32, R33,R34,R35,R36,R37, R38,R39,R40,R41,R42, R43,R44,R45,R46,R47, R48,R49,R50,R51,R52, R53,R54,R55,R56,R57, R58,R59,R60,R61,R62, R63,R72,R73,R74,R77, R80,R176,R177,R180,R181, R200,R201,R202	
47	0	1206(3216)	4	R	R204,R205,R206,R207	
48	33	0603(1608)	12	R	R2,R3,R5,R65,R85 R86,R87,R88,R95,R96 R97,R107	
59	49.9	0603(1608)	4	R	R89,R90,R91,R92	
50	75	0603(1608)	5	R	R84,R103,R104,R105,R106	
51	100	0603(1608)	1	R	R178	
52	270	0603(1608)	3	R	R155,R,156,R157	
53	330	0603(1608)	5	R	R144,145,R146,R147,R151	
54	390	0603(1608)	3	R	R158,R159,R160	
55	500	0603(1608)	2	R	R93 R94	
56	560	0603(1608)	4	R	R161,R162,R172,R174	
57	820	0603(1608)	1	R	R163	
58	1K	0603(1608)	10	R	R4,R7,R79,R82,R83 R152, R153,R154,R164,R168	
59	2K	0603(1608)	4	R	R66,R67,R69,R70	
60	3K	0603(1608)	1	R	R179	
61	2.2K	0603(1608)	1	R	R167	
62	4.7K	0603(1608)	50	R	R6,R64,R68,R71,R75, R76,R78,R81,R98,R99, R100,R101,R108,R109,R110,R111, R112,R113,R114,R115,R116,R117, R118,R119,R120,R121,R122,R123, R124,R125,R126,R127,R128,R129, R130,R131,R132,R133,R134,R135, R136,R137,R138,R139,R140,R141, R142,R143,R150,R166	
63	10K	0603(1608)	5	R	R102,R148,R149,R173,R175	
64	20K	0603(1608)	1	R	R171	

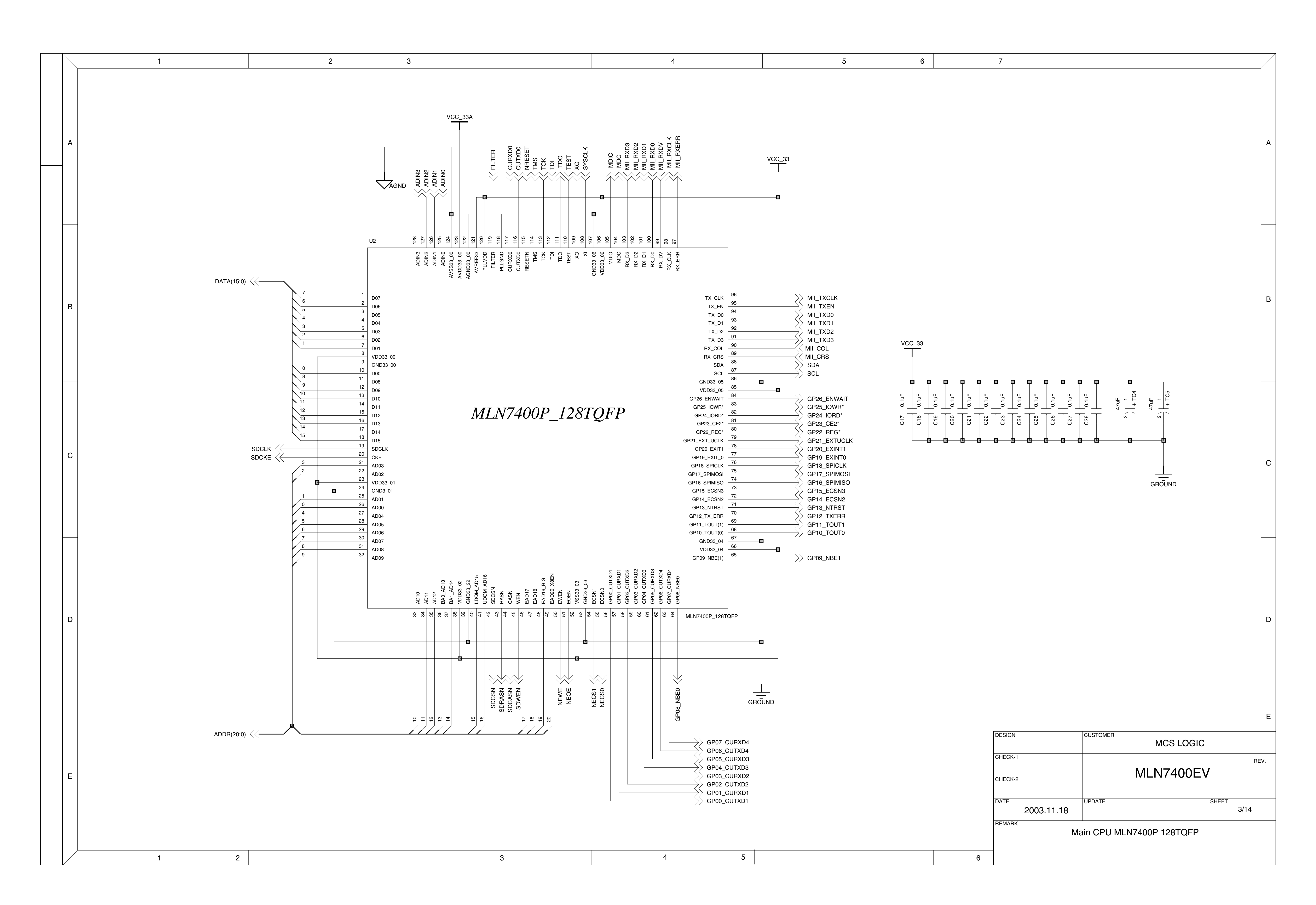
65	100K	0603(1608)	3	R	R165,R169,R170	
66	1M	0603(1608)	1	R	R1	
67	0.01uF_2kV	DIP	1		C56	
68	0.01uF	0603(1608)	9	C	C47,C57,C58,C59,C60, C61,C62,C83,C87	
69	0.1uF	0603(1608)	65	C	C1,C2,C3,C4,C5, C6,C7,C8,C9,C10, C11,C12,C15,C17,C18, C19,C20,C21,C22,C23, C24,C25,C26,C27,C28, C29,C32,C33,C34,C35, C36,C37,C38,C39,C40, C41,C42,C43,C44,C45, C46,C48,C50,C52,C63, C64,C65,C66,C79,C80, C81,C82,C85,C89,C92, C93,C94,C96,C97,C183, C184,C185,C186C187,C188	
70	1uF	0603(1608)	6	C	C51,C53,C54,C55,C90, C91	
71	20pF	0603(1608)	2	C	C13,C14	
72	22pF	0603(1608)	2	C	C30,C31	
73	27pF	0603(1608)	1	C	C49	
74	47pF	0603(1608)	1	C	C88	
75	100pF	0603(1608)	1	C	C95	
76	330pF	0603(1608)	12	C	C67,C68,C69,C70,C71, C72,C73,C74,C75,C76, C77,C78	
77	820pF	0603(1608)	1	C	C16	
78	1uF	SMD A(3216)	17	T/C	TC11,TC12,TC13,TC14,TC15TC16, TC17,TC18,TC19,TC20TC21,TC22, TC37,TC38,TC39 TC41, TC42	
79	2.2uF	SMD A(3216)	2	T/C	TC9,TC10	
80	3.3uF	SMD A(3216)	2	T/C	TC35,TC36	
81	10uF	SMD B(3528)	8	T/C	TC3,TC6,TC7,TC25,TC26, TC28,TC29,TC34	
82	22uF	SMD B(3528)	1	T/C	TC8	
83	47uF	SMD C(6032)	6	T/C	TC1,TC2,TC4,TC5,TC23, TC24	
84	100uF	SMD D(7343)	3	T/C	TC27,TC31,TC33	

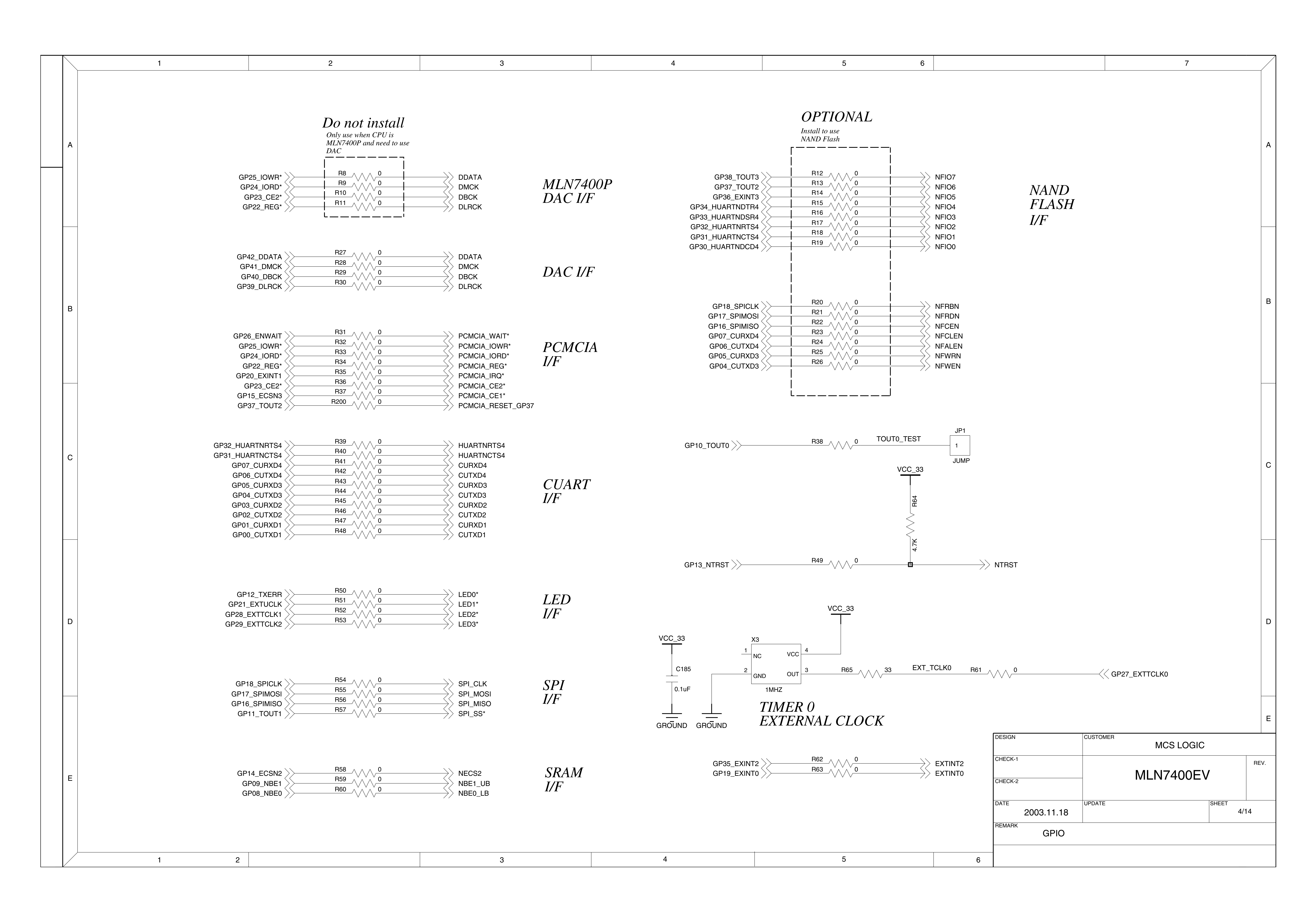
6.2 EVB7400 Schematic

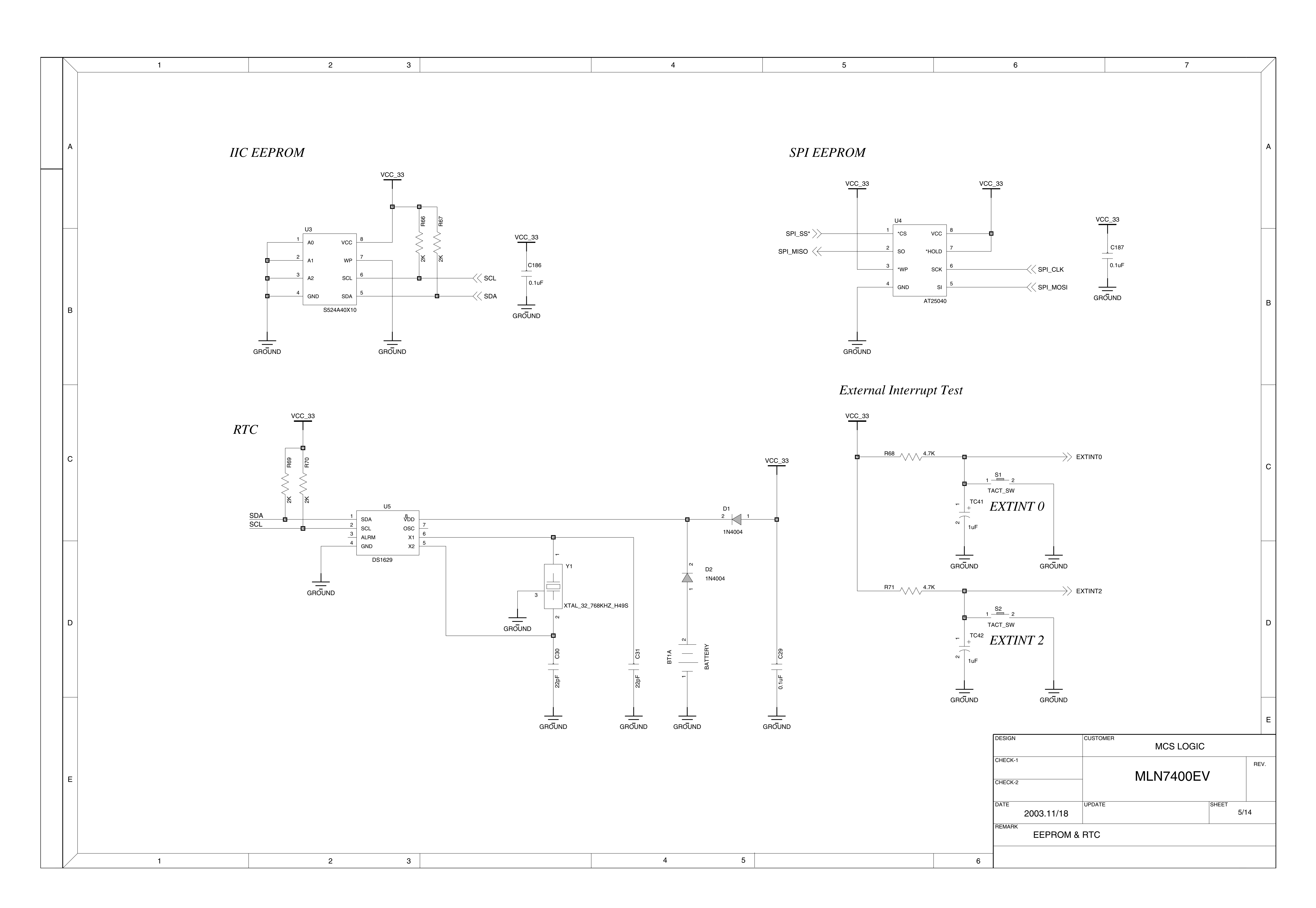


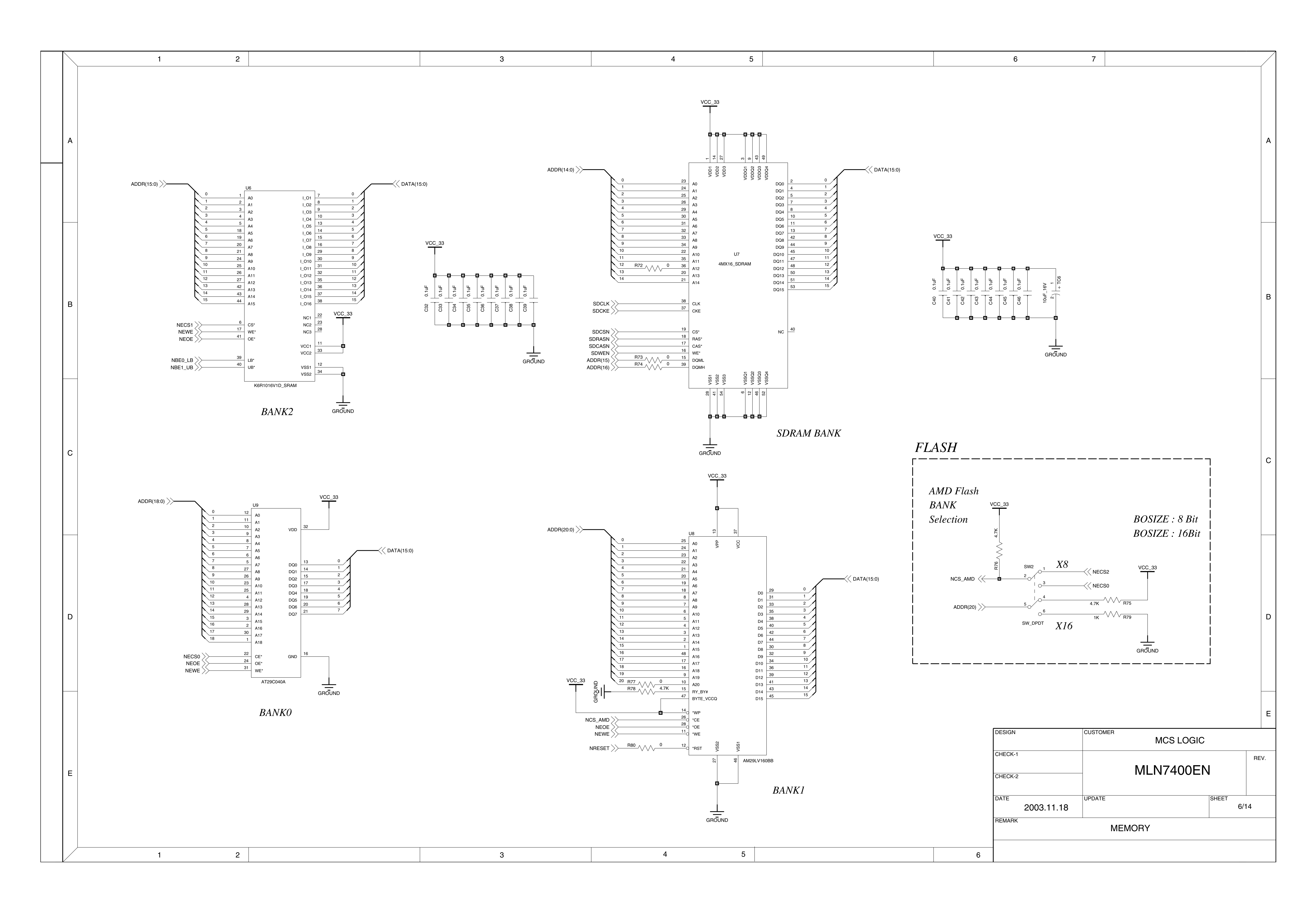
MLN7400 Evaluation Board
DESIGN
CUSTOMER
MCS LOGIC
CHECK-1
REV.
MLN7400EV
CHECK-2
DATE
2003.11.18
UPDATE
SHEET
1 / 14
REMARK
BLOCK DIAGRAM

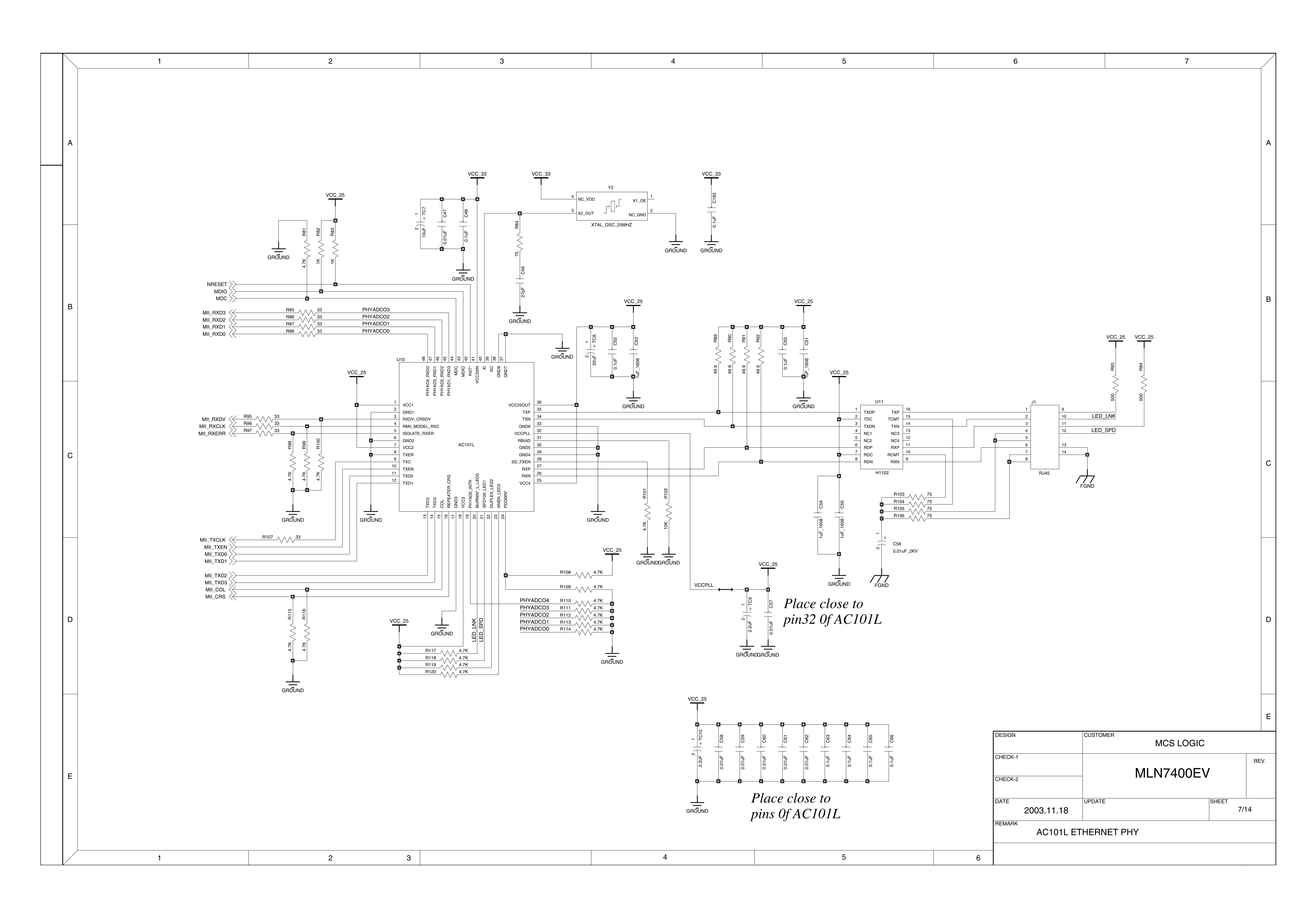

OPTIONAL
SYSTEM CLOCK
MLN7400_144LQFP
U1
DATA(15:0)
ADDR(20:0)
SDCLK
SDCKE
GP27_EXTTCLK0
GP28_EXTTCLK1
GP29_EXTTCLK2
GP30_HUARTNDCD4
FILTER
VCC_33
VCC_33A
AGND
GROUND
FGND
BEADS_100MHz
10MHz
10MHZ
TDO
TDI
TCK
TMS
TEST
SYSCLK
NRESET
XI
XO
ADIN0
ADIN1
ADIN2
ADIN3
MDIO
MDC
MII_RXD3
MII_RXD2
MII_RXD1
MII_RXD0
MII_RXDV
MII_RXCLK
MII_RXERR
MII_TXCLK
MII_TXEN
MII_TXD0
MII_TXD1
MII_TXD2
MII_TXD3
MII_COL
MII_CRS
GP38_TOUT3
GP37_TOUT2
GP36_EXINT3
GP35_EXINT2
SDA
SCL
GP26_ENWAIT
GP25_IOWR*
GP24_IORD*
GP23_CE2*
GP22_REG*
GP21_EXTUCLK
GP20_EXINT1
GP19_EXINT0
GP18_SPICLK
GP17_SPIMOSI
GP16_SPIMISO
GP15_ECSN3
GP14_ECSN2
GP13_NTRST
GP12_TXERR
GP11_TOUT1
GP10_TOUT0
GP09_NBE1
GP08_NBE0
GP07_CURXD4
GP06_CUTXD4
GP05_CURXD3
GP04_CUTXD3
GP03_CURXD2
GP02_CUTXD2
GP01_CURXD1
GP00_CUTXD1
SDCSN
SDRASN
SDCASN
SDWEN
GP31_HUARTNCTS4
GP32_HUARTNRTS4
NEWE
NEOE
GP33_HUARTNDSR4
GP34_HUARTNDTR4
NECS1
NECS0
FHOLE3.5
Endian Setting
ADDR(19)
SW1
SW_DPDT
BIG
LITTLE
DESIGN
CUSTOMER
MCS LOGIC
CHECK-1
CHECK-2
MLN7400EV
REV.
DATE
2003.11.18
UPDATE
SHEET
2/14
REMARK
Main CPU MLN7400


VCC_33A
AGND
ADIN3
ADIN2
ADIN1
ADIN0
FILTER
CURXD0
CUTXD0
NRESET
TMS
TCK
TDI
TDO
TEST
XO
SYSCLK
MDIO
MDC
MII_RXD3
MII_RXD2
MII_RXD1
MII_RXD0
MII_RXDV
MII_RXCLK
MII_RXERR
VCC_33
U2
DATA(15:0)
SDCLK
SDCKE
ADDR(20:0)
MLN7400P_128TQFP
MII_TXCLK
MII_TXEN
MII_TXD0
MII_TXD1
MII_TXD2
MII_TXD3
MII_COL
MII_CRS
SDA
SCL
GP26_ENWAIT
GP25_IOWR*
GP24_IORD*
GP23_CE2*
GP22_REG*
GP21_EXTUCLK
GP20_EXINT1
GP19_EXINT0
GP18_SPICLK
GP17_SPIMOSI
GP16_SPIMISO
GP15_ECSN3
GP14_ECSN2
GP13_NTRST
GP12_TXERR
GP11_TOUT1
GP10_TOUT0
GP09_NBE1
SDCSN
SDRASN
SDCASN
SDWEN
NEWE
NEOE
NECS1
NECS0
GP08_NBE0
GROUND
GP07_CURXD4
GP06_CUTXD4
GP05_CURXD3
GP04_CUTXD3
GP03_CURXD2
GP02_CUTXD2
GP01_CURXD1
GP00_CUTXD1
C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 0.1uF
TC4 TC5 47uF
DESIGN
CUSTOMER
MCS LOGIC
CHECK-1
CHECK-2
MLN7400EV
REV.
DATE
2003.11.18
UPDATE
SHEET
3/14
REMARK
Main CPU MLN7400P 128TQFP

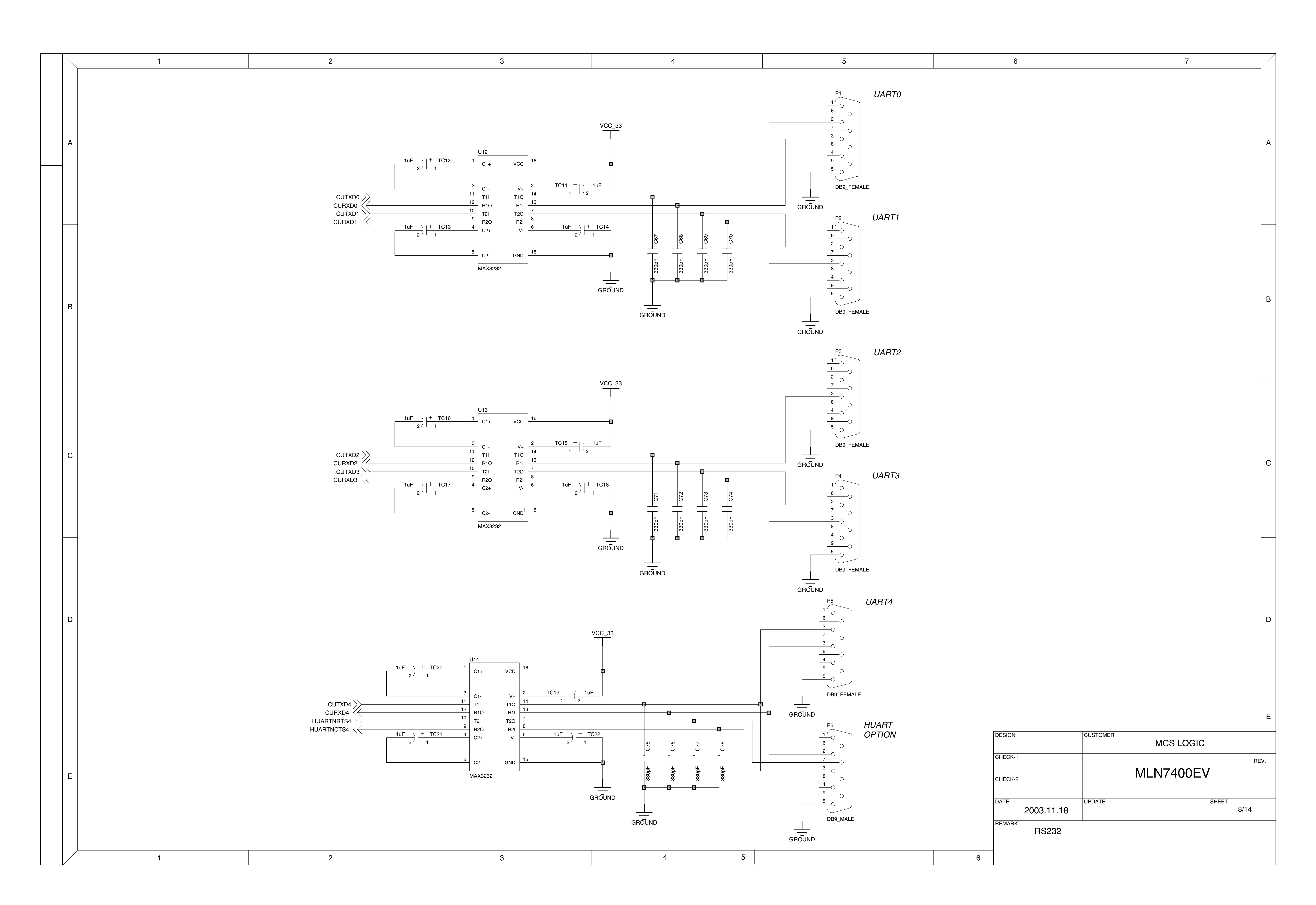

Do not install
Only use when CPU is MLN7400P and need to use DAC
GP25_IOWR* R8 0 DDATA
GP24_IORD* R9 0 DMCK
GP23_CE2* R10 0 DBCK
GP22_REG* R11 0 DLRCK
MLN7400P DAC I/F
GP42_DDATA R27 0 DDATA
GP41_DMCK R28 0 DMCK
GP40_DBCK R29 0 DBCK
GP39_DLRCK R30 0 DLRCK
DAC I/F
GP26_ENWAIT R31 0 PCMCIA_WAIT*
GP25_IOWR* R32 0 PCMCIA_IOWR*
GP24_IORD* R33 0 PCMCIA_IORD*
GP22_REG* R34 0 PCMCIA_REG*
GP20_EXINT1 R35 0 PCMCIA_IRQ*
GP23_CE2* R36 0 PCMCIA_CE2*
GP15_ECSN3 R37 0 PCMCIA_CE1*
GP37_TOUT2 R200 0 PCMCIA_RESET_GP37
PCMCIA I/F
GP32_HUARTNRTS4 R39 0 HUARTNRTS4
GP31_HUARTNCTS4 R40 0 HUARTNCTS4
GP07_CURXD4 R41 0 CURXD4
GP06_CUTXD4 R42 0 CUTXD4
GP05_CURXD3 R43 0 CURXD3
GP04_CUTXD3 R44 0 CUTXD3
GP03_CURXD2 R45 0 CURXD2
GP02_CUTXD2 R46 0 CUTXD2
GP01_CURXD1 R47 0 CURXD1
GP00_CUTXD1 R48 0 CUTXD1
CUART I/F
GP12_TXERR R50 0 LED0*
GP21_EXTUCLK R51 0 LED1*
GP28_EXTTCLK1 R52 0 LED2*
GP29_EXTTCLK2 R53 0 LED3*
LED I/F
GP18_SPICLK R54 0 SPI_CLK
GP17_SPIMOSI R55 0 SPI_MOSI
GP16_SPIMISO R56 0 SPI_MISO
GP11_TOUT1 R57 0 SPI_SS*
SPI I/F
GP14_ECSN2 R58 0 NECS2
GP09_NBE1 R59 0 NBE1_UB
GP08_NBE0 R60 0 NBE0_LB
SRAM I/F
OPTIONAL
Install to use NAND Flash
GP38_TOUT3 R12 0 NFIO7
GP37_TOUT2 R13 0 NFIO6
GP36_EXINT3 R14 0 NFIO5
GP34_HUARTNDTR4 R15 0 NFIO4
GP33_HUARTNDSR4 R16 0 NFIO3
GP32_HUARTNRTS4 R17 0 NFIO2
GP31_HUARTNCTS4 R18 0 NFIO1
GP30_HUARTNDCD4 R19 0 NFIO0
NAND FLASH I/F
GP18_SPICLK R20 0 NFRBN
GP17_SPIMOSI R21 0 NFRDN
GP16_SPIMISO R22 0 NFCEN
GP07_CURXD4 R23 0 NFCLEN
GP06_CUTXD4 R24 0 NFALEN
GP05_CURXD3 R25 0 NFWRN
GP04_CUTXD3 R26 0 NFWEN
GP10_TOUT0 R38 0 TOUT0_TEST JP1 1 JUMP
VCC_33 R64 4.7K
GP13_NTRST R49 0 NTRST
VCC_33
VCC_33 C185 0.1uF GROUND GROUND
X3 1 NC 2 GND VCC 4 OUT 3 1MHZ
R65 33 EXT_TCLK0 R61 0 GP27_EXTTCLK0
TIMER 0 EXTERNAL CLOCK
GP35_EXINT2 R62 0 EXTINT2
GP19_EXINT0 R63 0 EXTINT0
DESIGN
CUSTOMER MCS LOGIC
CHECK-1
CHECK-2
MLN7400EV
REV.
DATE 2003.11.18
UPDATE
SHEET 4/14
REMARK GPIO


IIC EEPROM
SPI EEPROM
VCC_33
U3
A0
A1
A2
GND
VCC
WP
SCL
SDA
S524A40X10
R66
R67
2K
SCL
SDA
C186
0.1uF
GROUND
U4
*CS
SO
*WP
GND
VCC
*HOLD
SCK
SI
AT25040
SPI_SS*
SPI_MISO
SPI_CLK
SPI_MOSI
C187
External Interrupt Test
R68
4.7K
EXTINT0
S1
TACT_SW
TC41
1uF
EXTINT 0
R71
EXTINT2
S2
TC42
EXTINT 2
RTC
R69
R70
U5
SDA
SCL
ALRM
GND
VDD
OSC
X1
X2
DS1629
Y1
XTAL_32_768KHZ_H49S
C30
22pF
C31
D1
1N4004
D2
BT1A
BATTERY
C29
DESIGN
CUSTOMER
MCS LOGIC
CHECK-1
CHECK-2
MLN7400EV
REV.
DATE
2003.11/18
UPDATE
SHEET
5/14
REMARK
EEPROM & RTC

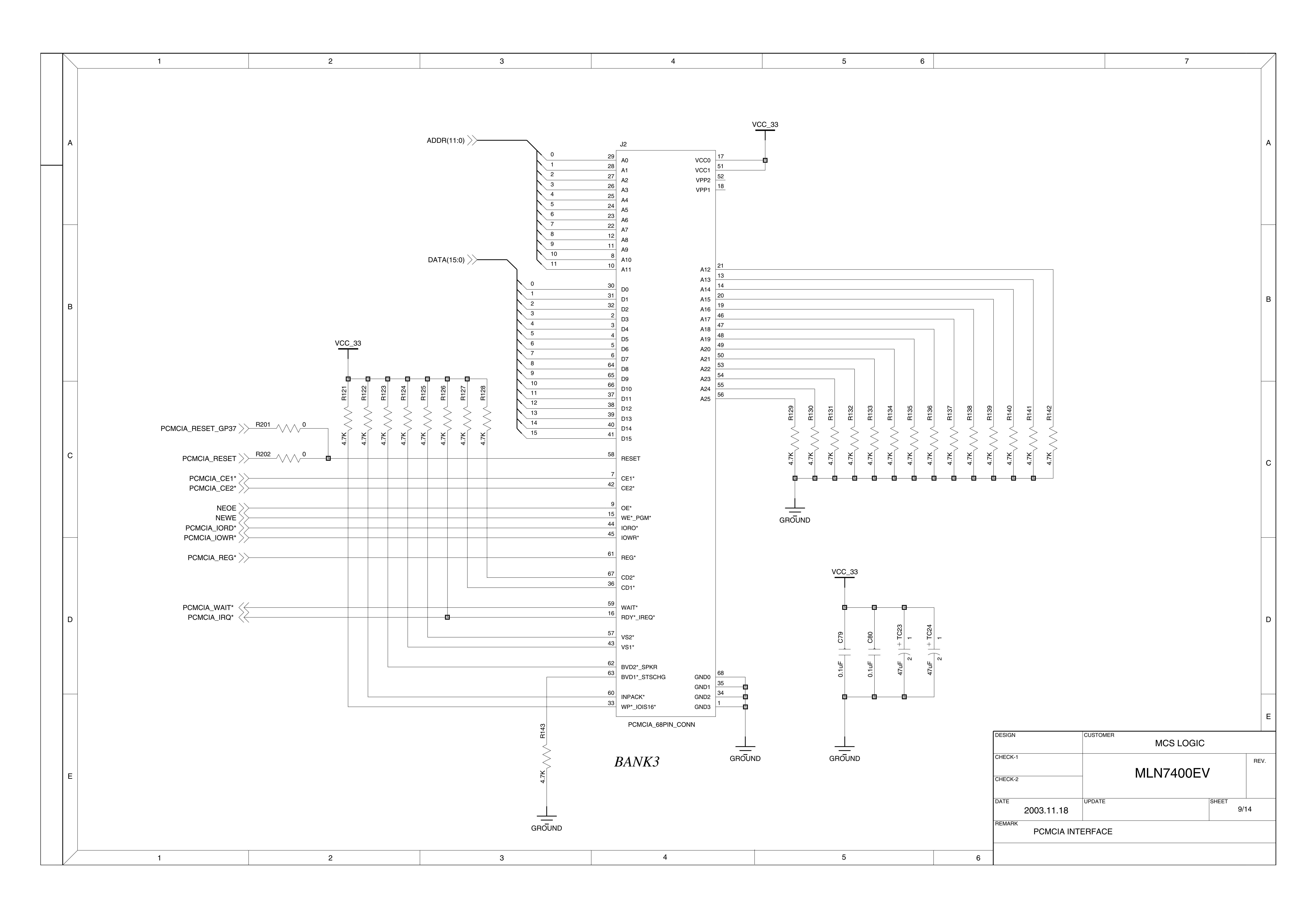

BANK2
U6
K6R1016V1D_SRAM
ADDR(15:0)
DATA(15:0)
NECS1
NEWE
NEOE
NBE0_LB
NBE1_UB
VCC_33
GROUND
U7
4MX16_SDRAM
ADDR(14:0)
SDCLK
SDCKE
SDCSN
SDRASN
SDCASN
SDWEN
ADDR(15)
ADDR(16)
R72
R73
R74
SDRAM BANK
FLASH
AMD Flash
BANK
Selection
BOSIZE : 8 Bit
BOSIZE : 16Bit
X8
X16
SW2
SW_DPDT
NCS_AMD
ADDR(20)
NECS2
NECS0
R75
R76
R79
BANK0
U9
AT29C040A
ADDR(18:0)
NECS0
NEOE
NEWE
BANK1
U8
AM29LV160BB
ADDR(20:0)
NCS_AMD
NEOE
NEWE
NRESET
R77
R78
R80
DESIGN
CUSTOMER
MCS LOGIC
CHECK-1
CHECK-2
MLN7400EN
REV.
DATE
2003.11.18
UPDATE
SHEET
6/14
REMARK
MEMORY



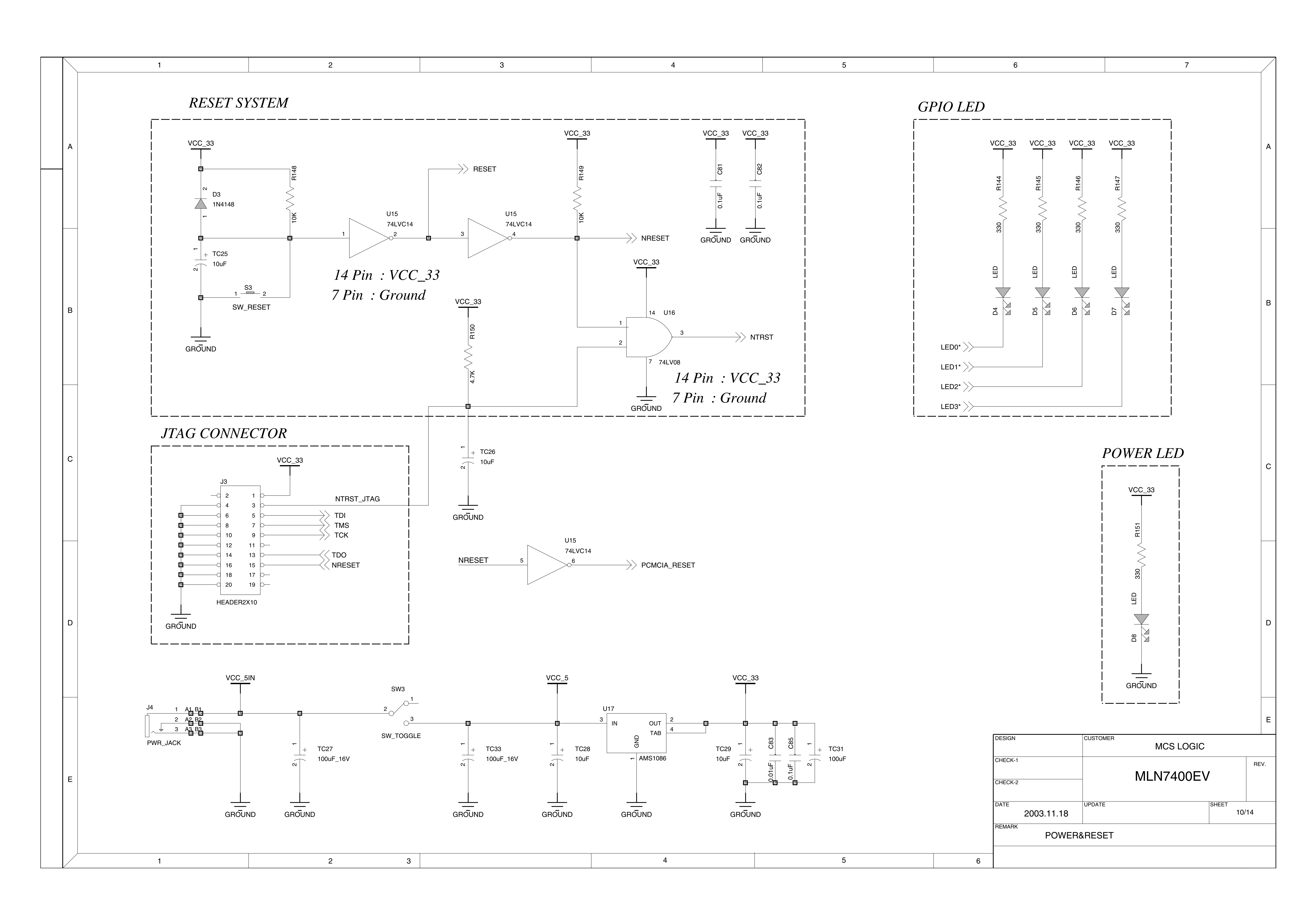
VCC_33
VCC_25
Y2
NC_VDD
X1_OE
X2_OUT
NC_GND
XTAL_OSC_25MHZ
GROUND
NRESET
MDIO
MDC
MII_RXD3
MII_RXD2
MII_RXD1
MII_RXD0
PHYADCO3
PHYADCO2
PHYADCO1
PHYADCO0
U10
AC101L
MII_RXDV
MII_RXCLK
MII_RXERR
VCC1
GND1
RXDV_CRSDV
RMII_MODEL_RXC
ISOLATE_RXER
GND2
VCC2
TXER
TXC
TXEN
TXD0
TXD1
VCC25OUT
TXP
TXN
GND6
VCCPLL
RBIAS
GND5
GND4
SD_FXEN
RXP
RXN
VCC4
PHYAD4_RXD0
PHYAD3_RXD1
PHYAD2_RXD2
PHYAD1_RXD3
MDC
MDIO
RST
VCC33IN
XI
XO
GND8
GND7
TXD2
TXD3
COL
REPEATER_CRS
GND3
VCC3
PHYAD0_INTR
BURNIN_LED0
SPD100_LED1
DUPLEX_LED2
ANEN_LED3
PDOWN
MII_TXCLK
MII_TXEN
MII_TXD0
MII_TXD1
MII_TXD2
MII_TXD3
MII_COL
MII_CRS
LED_LNK
LED_SPD
PHYADCO4
VCCPLL
U11
H1102
TXDP
TDC
TXDN
NC1
NC2
RDP
RDC
RDN
TXP
TCMT
TXN
NC3
NC4
RXP
RCMT
RXN
J1
RJ45
FGND
C56
0.01uF_2KV
Place close to
pin32 0f AC101L
Place close to
pins 0f AC101L
DESIGN
CUSTOMER
MCS LOGIC
CHECK-1
CHECK-2
MLN7400EV
REV.
DATE
2003.11.18
UPDATE
SHEET
7/14
REMARK
AC101L ETHERNET PHY



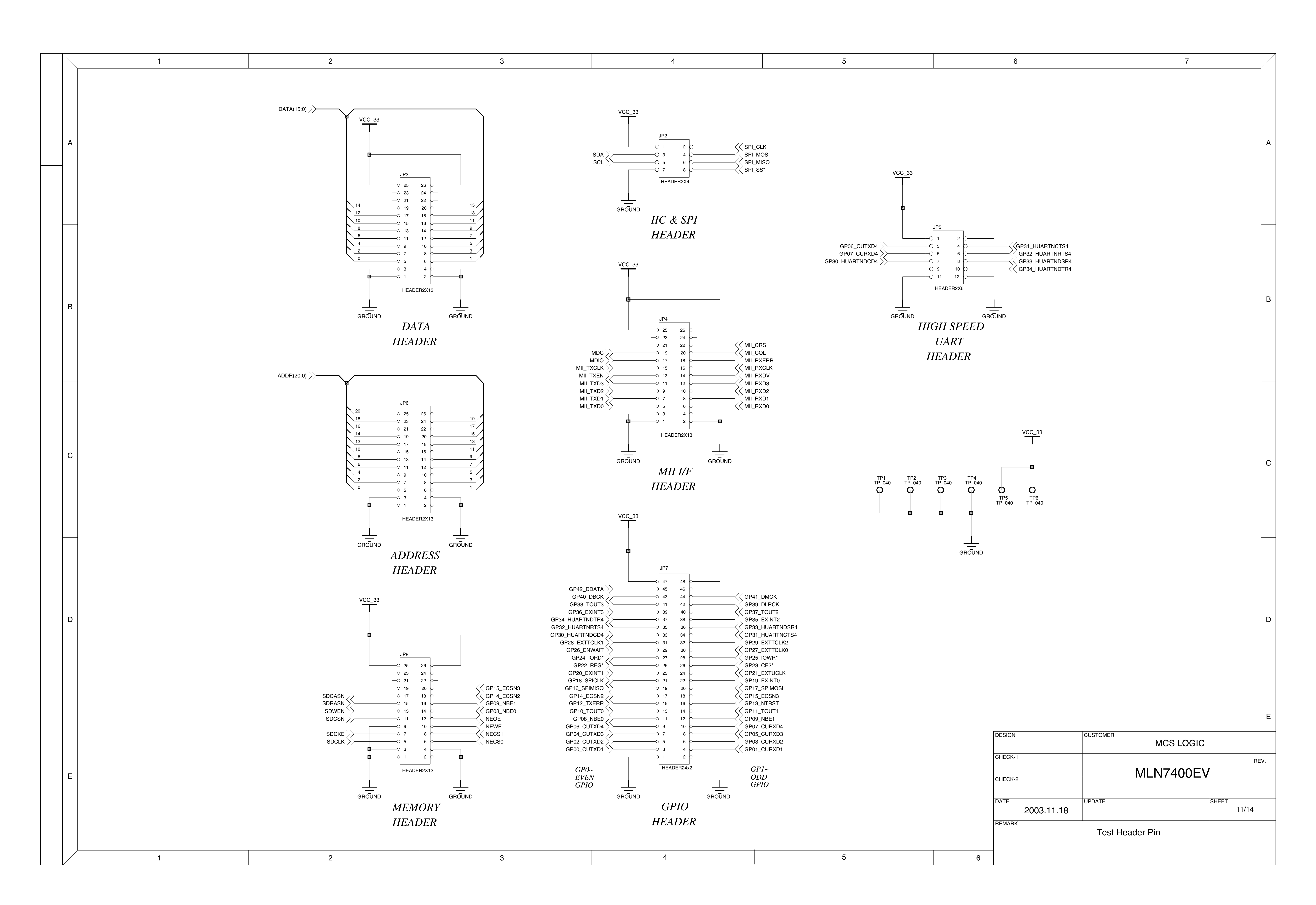
UART0
UART1
UART2
UART3
UART4
HUART OPTION
U12
U13
U14
MAX3232
VCC_33
GROUND
CUTXD0
CURXD0
CUTXD1
CURXD1
CUTXD2
CURXD2
CUTXD3
CURXD3
CUTXD4
CURXD4
HUARTNRTS4
HUARTNCTS4
P1
P2
P3
P4
P5
P6
DB9_FEMALE
DB9_MALE
330pF
1uF
DESIGN
CUSTOMER
MCS LOGIC
CHECK-1
CHECK-2
MLN7400EV
REV.
DATE
2003.11.18
UPDATE
SHEET
8/14
REMARK
RS232

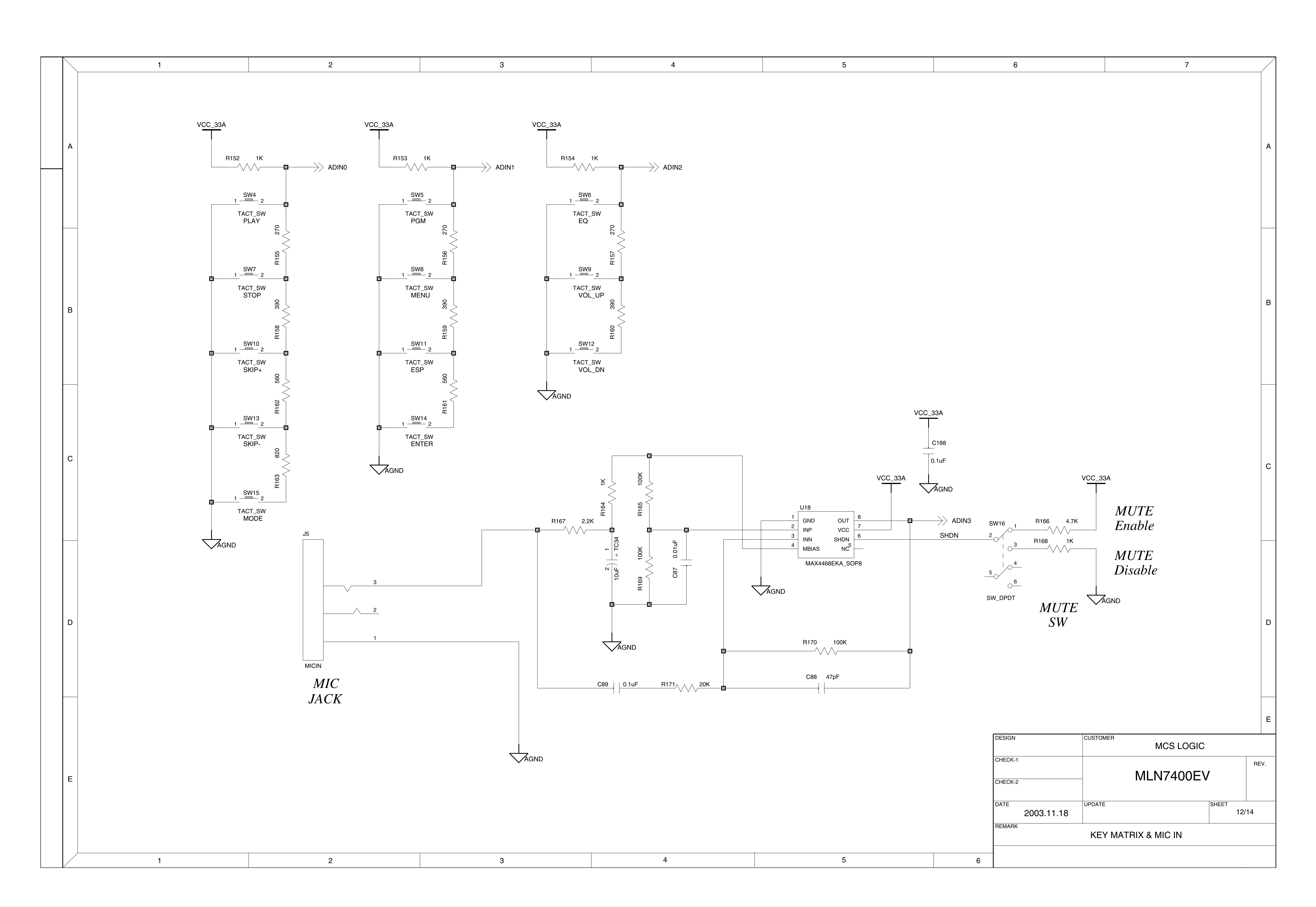


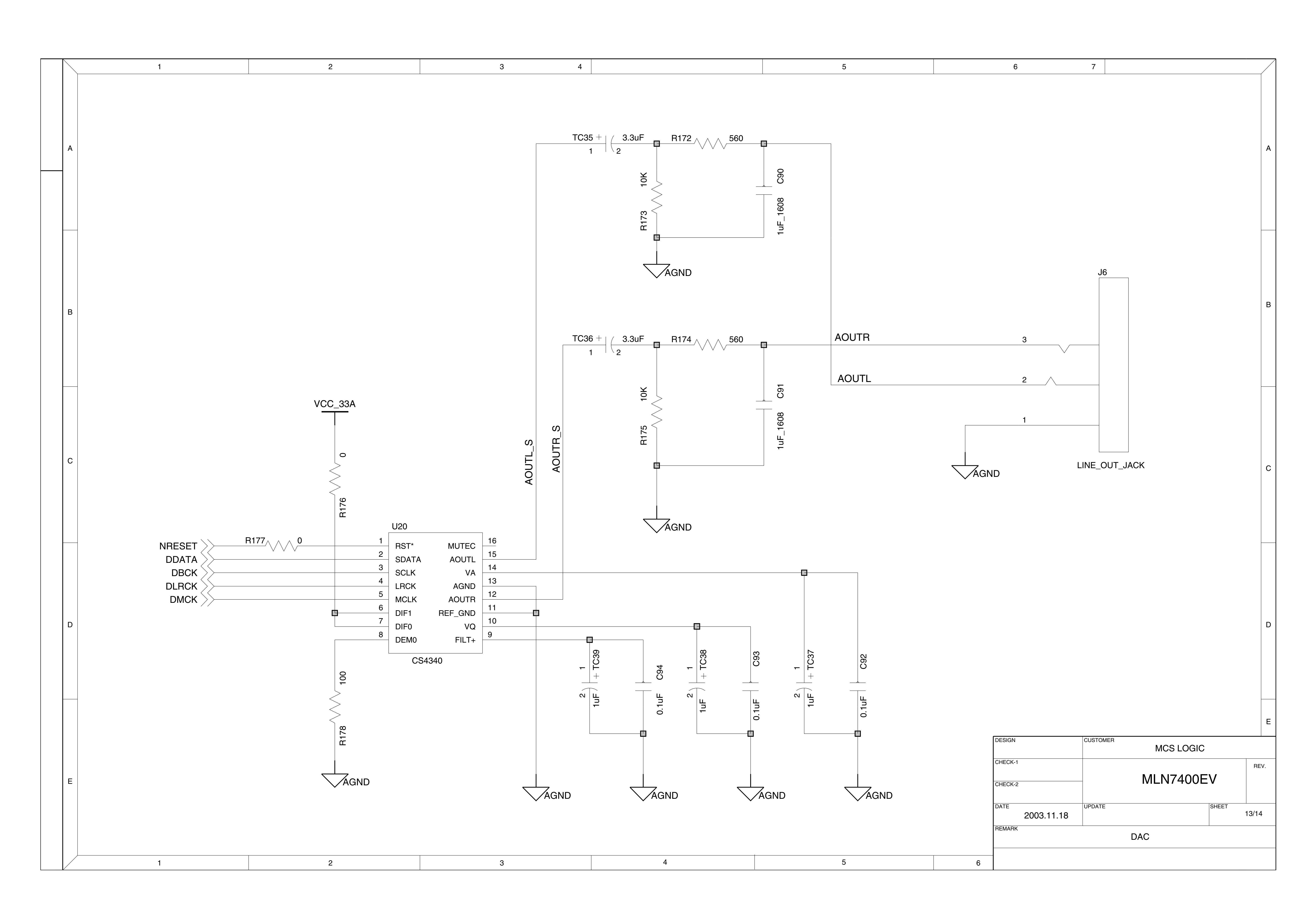
ADDR(11:0)
DATA(15:0)
J2
VCC_33
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15
VCC0 VCC1 VPP2 VPP1
A12 A13 A14 A15 A16 A17 A18 A19 A20 A21 A22 A23 A24 A25
PCMCIA_RESET_GP37
R201 0
PCMCIA_RESET
R202 0
PCMCIA_CE1*
PCMCIA_CE2*
NEOE
NEWE
PCMCIA_IORD*
PCMCIA_IOWR*
PCMCIA_REG*
PCMCIA_WAIT*
PCMCIA_IRQ*
R121 R122 R123 R124 R125 R126 R127 R128 4.7K
RESET
CE1*
CE2*
OE*
WE*_PGM*
IORD*
IOWR*
REG*
CD2*
CD1*
WAIT*
RDY*_IREQ*
VS2*
VS1*
BVD2*_SPKR
BVD1*_STSCHG
INPACK*
WP*_IOIS16*
GND0 GND1 GND2 GND3
PCMCIA_68PIN_CONN
R129 R130 R131 R132 R133 R134 R135 R136 R137 R138 R139 R140 R141 R142 4.7K
GROUND
R143 4.7K
BANK3
C79 0.1uF
C80 0.1uF
TC23 47uF
TC24 47uF
DESIGN
CUSTOMER
MCS LOGIC
CHECK-1
CHECK-2
MLN7400EV
REV.
DATE
2003.11.18
UPDATE
SHEET
9/14
REMARK
PCMCIA INTERFACE

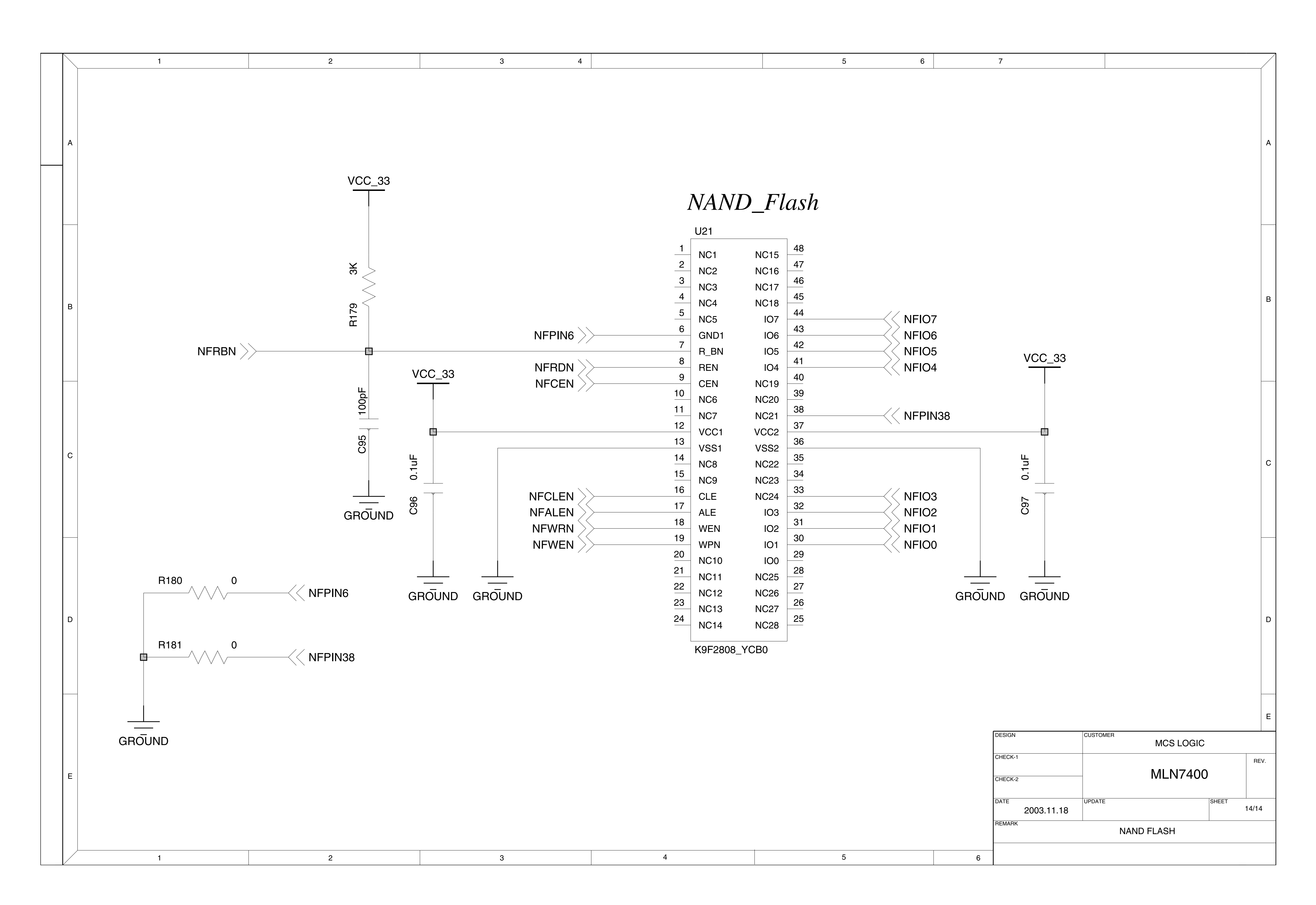


RESET SYSTEM
VCC_33
R148
10K
D3
1N4148
TC25
10uF
S3
SW_RESET
GROUND
U15
74LVC14
RESET
NRESET
R149
C81
0.1uF
C82
14 Pin : VCC_33
7 Pin : Ground
R150
4.7K
U16
74LV08
NTRST
GPIO LED
R144
R145
R146
R147
330
LED
D4
D5
D6
D7
LED0*
LED1*
LED2*
LED3*
JTAG CONNECTOR
J3
NTRST_JTAG
TDI
TMS
TCK
TDO
HEADER2X10
TC26
POWER LED
R151
D8
PCMCIA_RESET
VCC_5IN
J4
PWR_JACK
TC27
100uF_16V
SW3
SW_TOGGLE
VCC_5
TC33
TC28
U17
AMS1086
IN
OUT
TAB
GND
TC29
C83
0.01uF
C85
TC31
100uF
DESIGN
CUSTOMER
MCS LOGIC
CHECK-1
CHECK-2
MLN7400EV
REV.
DATE
2003.11.18
UPDATE
SHEET
10/14
REMARK
POWER&RESET


DATA(15:0)
VCC_33
JP3
HEADER2X13
GROUND
DATA
HEADER
ADDR(20:0)
JP6
HEADER2X13
ADDRESS
HEADER
JP8
SDCASN
SDRASN
SDWEN
SDCSN
SDCKE
SDCLK
GP15_ECSN3
GP14_ECSN2
GP09_NBE1
GP08_NBE0
NEOE
NEWE
NECS1
NECS0
MEMORY
HEADER
JP2
SDA
SCL
SPI_CLK
SPI_MOSI
SPI_MISO
SPI_SS*
HEADER2X4
IIC & SPI
HEADER
JP4
MDC
MDIO
MII_TXCLK
MII_TXEN
MII_TXD3
MII_TXD2
MII_TXD1
MII_TXD0
MII_CRS
MII_COL
MII_RXERR
MII_RXCLK
MII_RXDV
MII_RXD3
MII_RXD2
MII_RXD1
MII_RXD0
MII I/F
HEADER
JP7
GP42_DDATA
GP40_DBCK
GP38_TOUT3
GP36_EXINT3
GP34_HUARTNDTR4
GP32_HUARTNRTS4
GP30_HUARTNDCD4
GP28_EXTTCLK1
GP26_ENWAIT
GP24_IORD*
GP22_REG*
GP20_EXINT1
GP18_SPICLK
GP16_SPIMISO
GP14_ECSN2
GP12_TXERR
GP10_TOUT0
GP08_NBE0
GP06_CUTXD4
GP04_CUTXD3
GP02_CUTXD2
GP00_CUTXD1
GP41_DMCK
GP39_DLRCK
GP37_TOUT2
GP35_EXINT2
GP33_HUARTNDSR4
GP31_HUARTNCTS4
GP29_EXTTCLK2
GP27_EXTTCLK0
GP25_IOWR*
GP23_CE2*
GP21_EXTUCLK
GP19_EXINT0
GP17_SPIMOSI
GP15_ECSN3
GP13_NTRST
GP11_TOUT1
GP09_NBE1
GP07_CURXD4
GP05_CURXD3
GP03_CURXD2
GP01_CURXD1
HEADER24x2
GP0~
EVEN
GPIO
GP1~
ODD
GPIO
GPIO
HEADER
JP5
GP06_CUTXD4
GP07_CURXD4
GP30_HUARTNDCD4
GP31_HUARTNCTS4
GP32_HUARTNRTS4
GP33_HUARTNDSR4
GP34_HUARTNDTR4
HEADER2X6
HIGH SPEED
UART
HEADER
TP1 TP_040
TP2 TP_040
TP3 TP_040
TP4 TP_040
TP5 TP_040
TP6 TP_040
DESIGN
CUSTOMER
MCS LOGIC
CHECK-1
CHECK-2
MLN7400EV
REV.
DATE
2003.11.18
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SHEET
11/14
REMARK
Test Header Pin


VCC_33A
R152 1K
ADIN0
SW4 TACT_SW PLAY
SW7 TACT_SW STOP
SW10 TACT_SW SKIP+
SW13 TACT_SW SKIP-
SW15 TACT_SW MODE
R155 270
R158 390
R162 560
R163 820
AGND
R153 1K
ADIN1
SW5 TACT_SW PGM
SW8 TACT_SW MENU
SW11 TACT_SW ESP
SW14 TACT_SW ENTER
R156 270
R159 390
R161 560
R154 1K
ADIN2
SW6 TACT_SW EQ
SW9 TACT_SW VOL_UP
SW12 TACT_SW VOL_DN
R157 270
R160 390
C188 0.1uF
U18
GND INP INN MBIAS OUT VCC SHDN NC
MAX4468EKA_SOP8
ADIN3
SHDN
SW16
SW_DPDT
R166 4.7K
R168 1K
MUTE Enable
MUTE Disable
MUTE SW
R167 2.2K
R164 1K
R165 100K
R169 100K
TC34 10uF
C87 0.01uF
R170 100K
C89 0.1uF
R171 20K
C88 47pF
J5
MICIN
MIC JACK
DESIGN
CUSTOMER
MCS LOGIC
CHECK-1
CHECK-2
MLN7400EV
REV.
DATE
2003.11.18
UPDATE
SHEET
12/14
REMARK
KEY MATRIX & MIC IN


TC35
3.3uF
R172
560
10K
R173
C90
1uF_1608
AGND
J6
TC36
3.3uF
R174
560
AOUTR
AOUTL
10K
R175
C91
1uF_1608
LINE_OUT_JACK
VCC_33A
AOUTL_S
AOUTR_S
0
R176
U20
NRESET
DDATA
DBCK
DLRCK
DMCK
R177
0
RST*
SDATA
SCLK
LRCK
MCLK
DIF1
DIF0
DEM0
MUTEC
AOUTL
VA
AGND
AOUTR
REF_GND
VQ
FILT+
CS4340
100
R178
TC39
C94
1uF
0.1uF
TC38
C93
1uF
0.1uF
TC37
C92
1uF
0.1uF
DESIGN
CUSTOMER
MCS LOGIC
CHECK-1
CHECK-2
MLN7400EV
REV.
DATE
2003.11.18
UPDATE
SHEET
13/14
REMARK
DAC



NAND_Flash
U21
K9F2808_YCB0
1 NC1
2 NC2
3 NC3
4 NC4
5 NC5
6 GND1
7 R_BN
8 REN
9 CEN
10 NC6
11 NC7
12 VCC1
13 VSS1
14 NC8
15 NC9
16 CLE
17 ALE
18 WEN
19 WPN
20 NC10
21 NC11
22 NC12
23 NC13
24 NC14
48 NC15
47 NC16
46 NC17
45 NC18
44 IO7
43 IO6
42 IO5
41 IO4
40 NC19
39 NC20
38 NC21
37 VCC2
36 VSS2
35 NC22
34 NC23
33 NC24
32 IO3
31 IO2
30 IO1
29 IO0
28 NC25
27 NC26
26 NC27
25 NC28
NFPIN6
NFRBN
NFRDN
NFCEN
NFCLEN
NFALEN
NFWRN
NFWEN
NFIO7
NFIO6
NFIO5
NFIO4
NFPIN38
NFIO3
NFIO2
NFIO1
NFIO0
VCC_33
R179
3K
C95
100pF
C96
0.1uF
C97
0.1uF
GROUND
R180
0
NFPIN6
R181
0
NFPIN38
DESIGN
CUSTOMER
MCS LOGIC
CHECK-1
CHECK-2
MLN7400
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SHEET
14/14
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NAND FLASH